11091 PS6

Advanced SMPS Applications using the dsPIC® DSC SMPS Family

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Class Objective

- **When you finish this class you will:**
  - Understand design considerations for a High Power Converter
  - Know how to implement digital control loops using the dsPIC® DSC
  - Understand the benefits of Digital Power Conversion
  - View a demonstration of the AC/DC Reference Design

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Agenda

- **Overview of AC/DC Reference Design**
- **AC/DC Reference Design Architecture**
- **Power Factor Correction**
  - PFC Control Software
- **Zero Voltage Transition**
  - ZVT Control Software
- **Multi-phase Buck Converters**
  - Multi-phase Buck Control Software
- **Enhanced Features**

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Overview of the AC/DC Reference Design

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Overview of AC/DC Reference Design

- **Total Output Power Rating of 350 W**
- **Multiple DC Outputs:**
  - 3.3V, 69A (max)
  - 5V, 23A (max)
  - 12V, 28A (max)
- **Universal Operating Voltage**
  - 85V – 265V AC, 45-65 Hz
- **Digital PFC Implementation**
  - PF > 0.98

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Overview of AC/DC Reference Design

- Automatic Fault Handling
- Flexible Start-up Capability
- Remote Power Management Capability
- Full Digital Control

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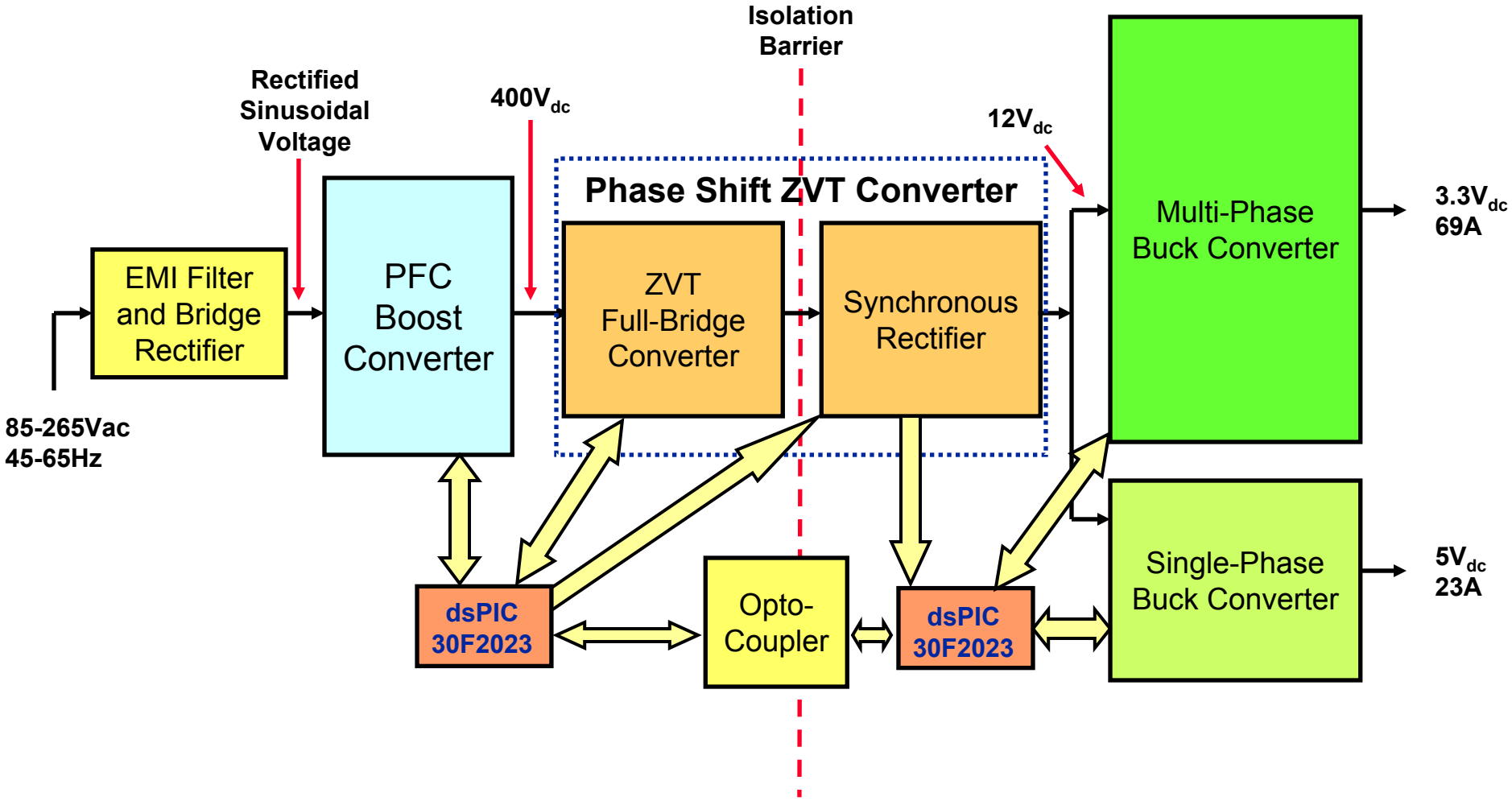
AC/DC Reference Design Block Diagram



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dsPIC® DSC SMPS Features

- **30 MIPS MCU + DSP core**
- **Intelligent Power Peripherals**
  - High Speed A/D: 10-bit, 2 MSPS
  - High Resolution PWM – 1.05ns
  - High Speed Analog Comparators
- **Internal Fast RC oscillator + PLL**
- **Small footprint package - 6 x 6 mm**
- **Flash-based controller**
- **CodeGuard™ Security Enabled**
- **Extended Temp (125°C) Operation**
- **Additional Information in 11089_PS4**

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AC/DC Reference Design Architecture

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Considerations for Choice of Architecture

- Number of Stages
- Choice of PFC Topology
- Switching Methodology
- Output Isolation requirements
- Requirements of Output Stage

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Considerations for Choice of Architecture

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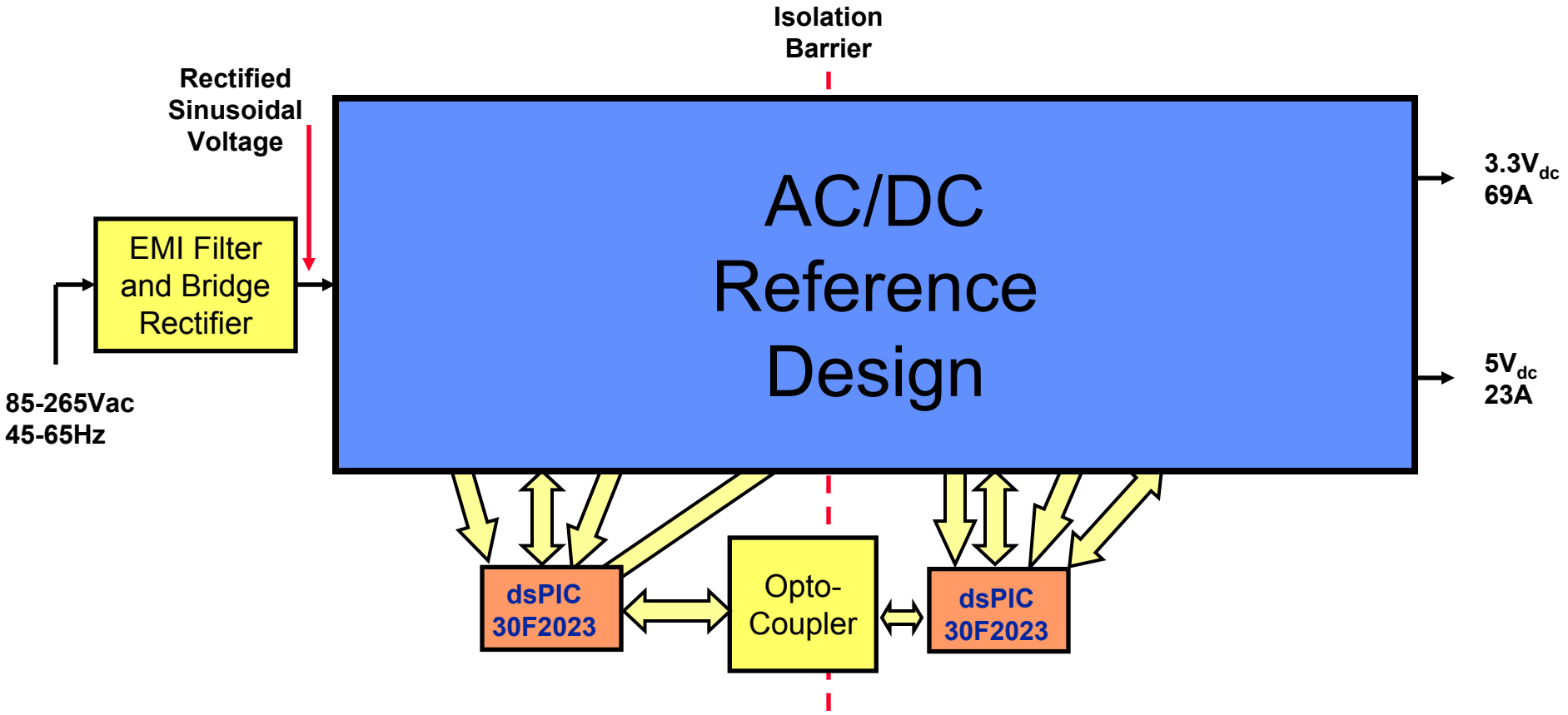
Multi-Stage Architecture



- **Multi-stage design simplifies design of each stage**

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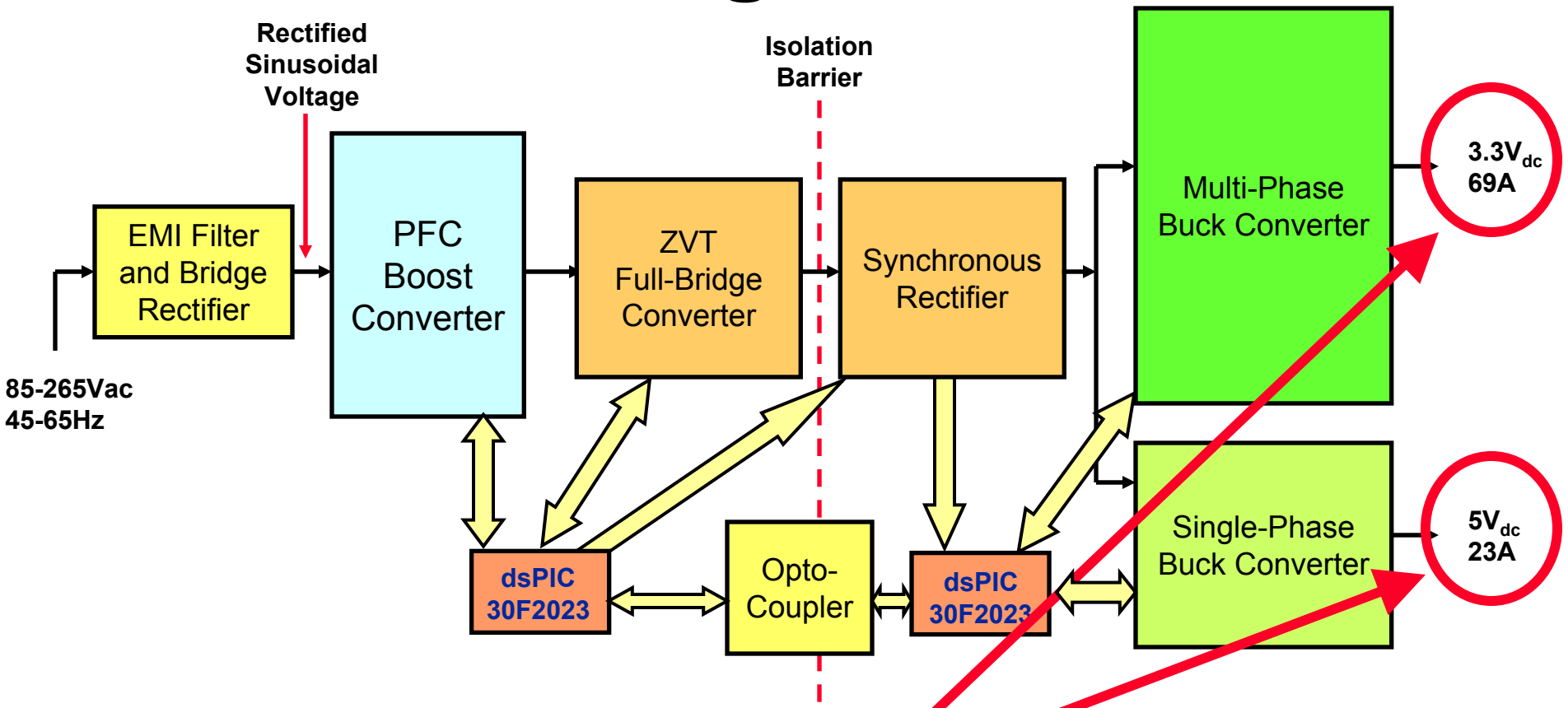
Multi-Stage Architecture



- **Multiple Outputs and multiple loads can be controlled Independently**

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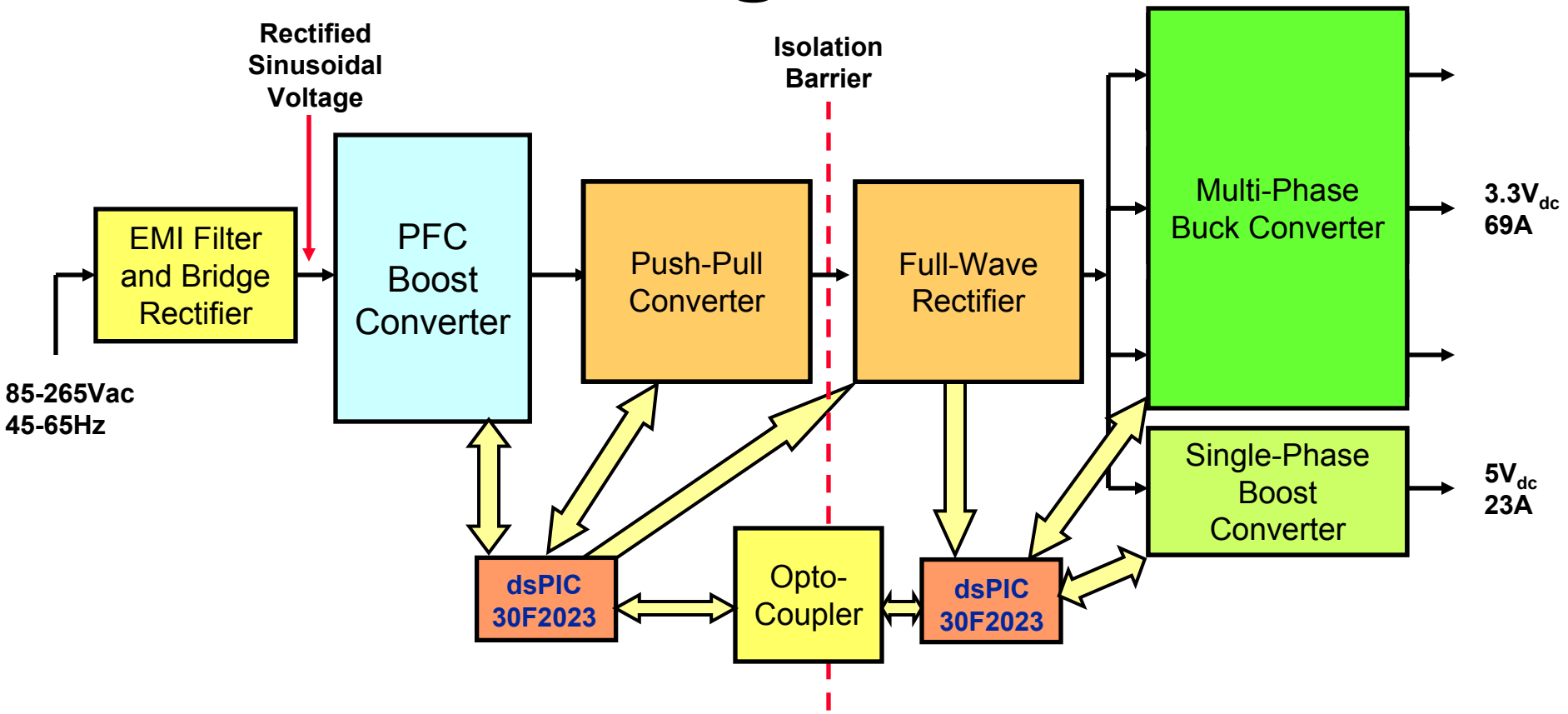
Multi-Stage Architecture



- **Modular Architecture enables swapping of stages with drop-in topologies**

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Considerations for Choice of Architecture

- Number of Stages
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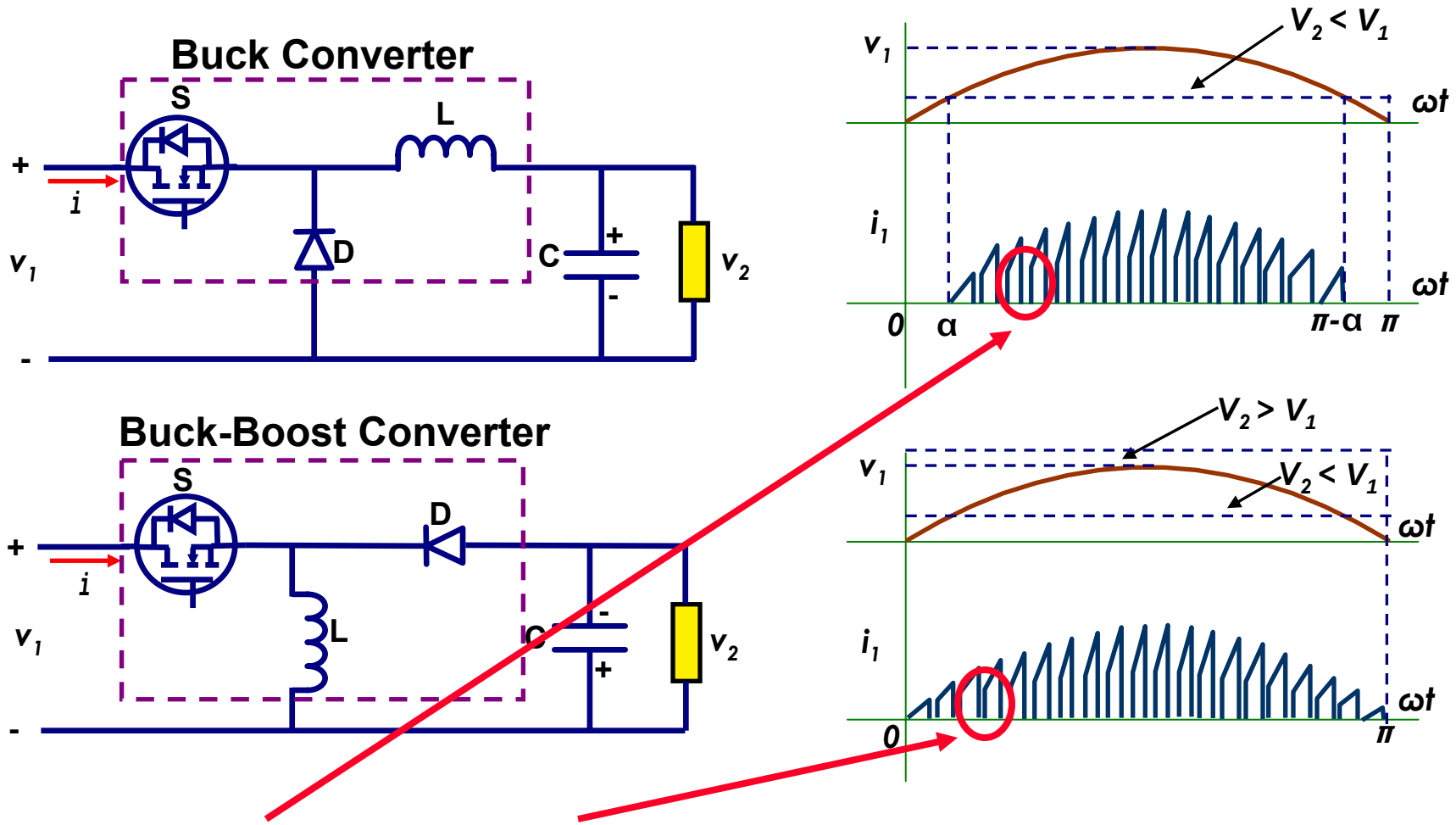
Choice of PFC Topology



- **Buck and Buck-Boost Topologies operate with discontinuous Current**

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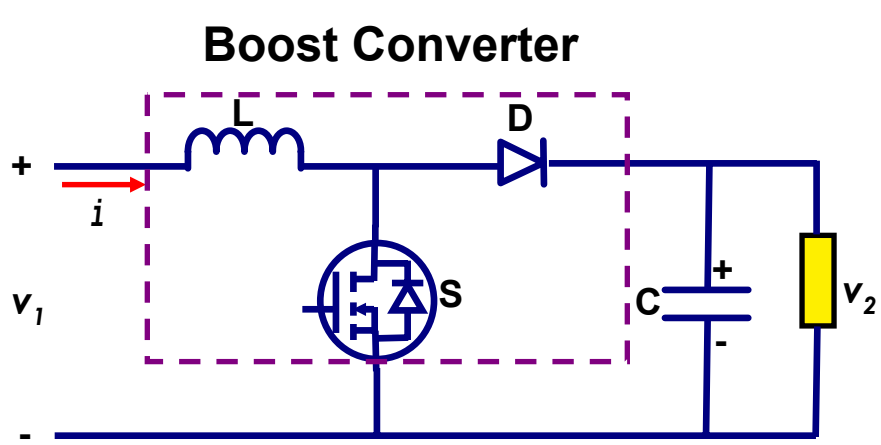
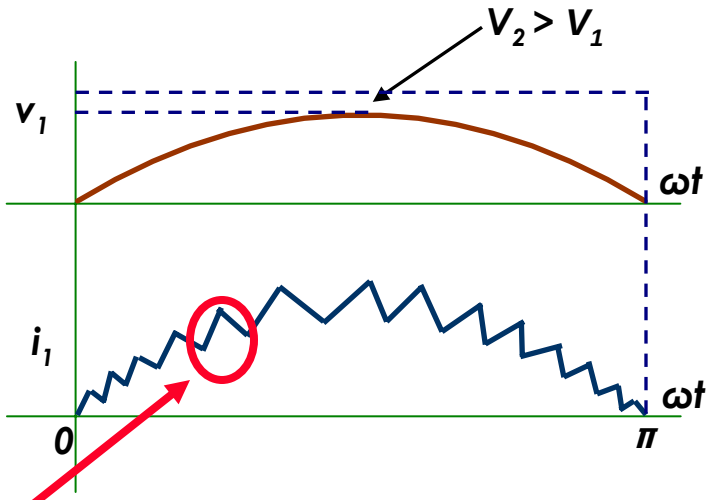
Why PFC Boost Converter?





- **Boost Converter operates with continuous input current at high loads**

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Considerations for Choice of Architecture

- Number of Stages
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Choice of Switching Methodology

Hard Switching	Soft Switching
Fixed Frequency Operation	Variable/Fixed Frequency Operation
Fewer Components Required	More Components Required
Simpler Control	Complex Control
High Switching Losses	Low Switching Losses
Used in Designs with Low Power and Low Performance Requirements	Used in Designs with High Power and High Performance Requirements

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Considerations for Choice of Architecture

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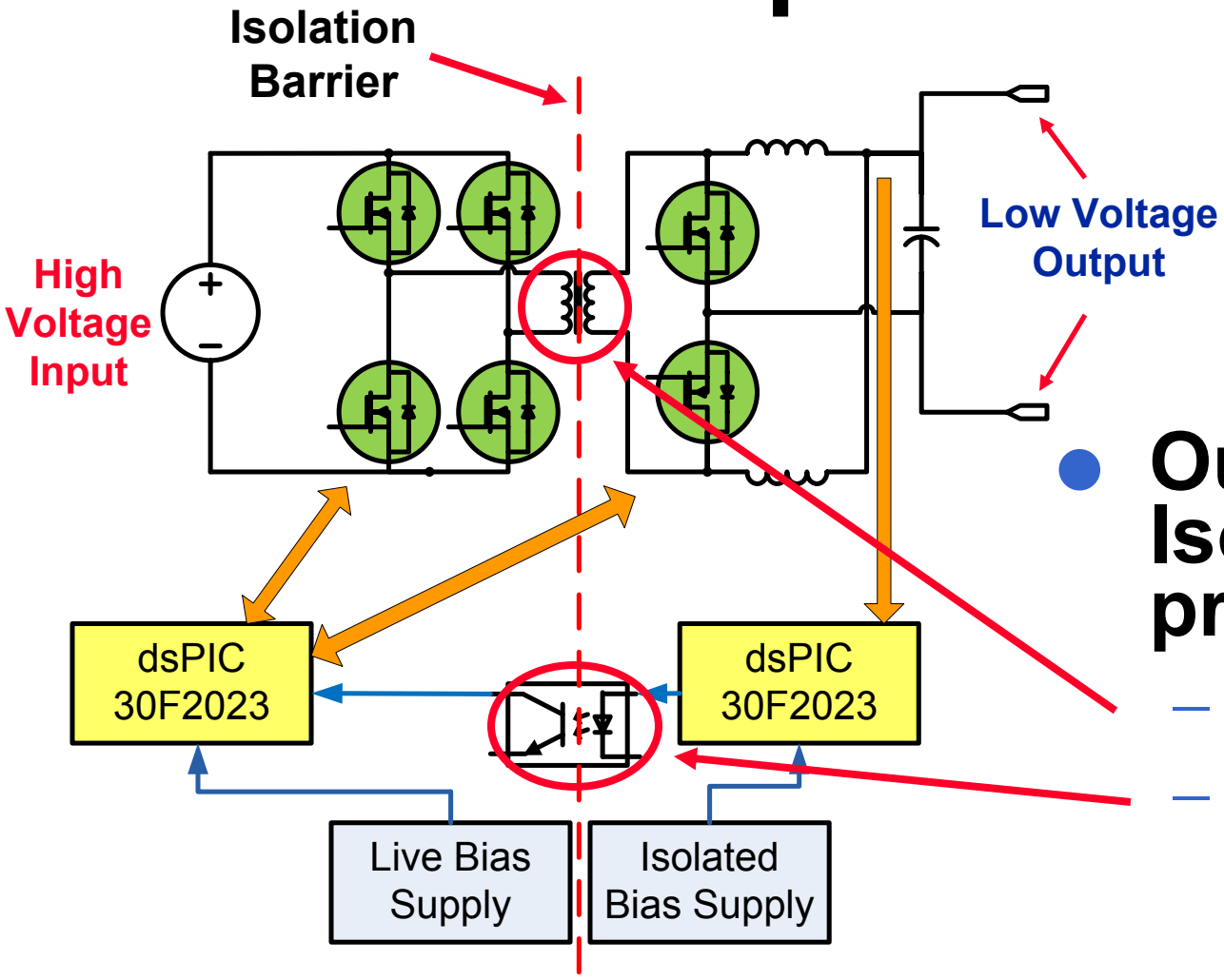
Output Isolation and Safety Requirements



- **Output Isolation is provided by:**
  - Transformers
  - Optocouplers

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Considerations for Choice of Architecture

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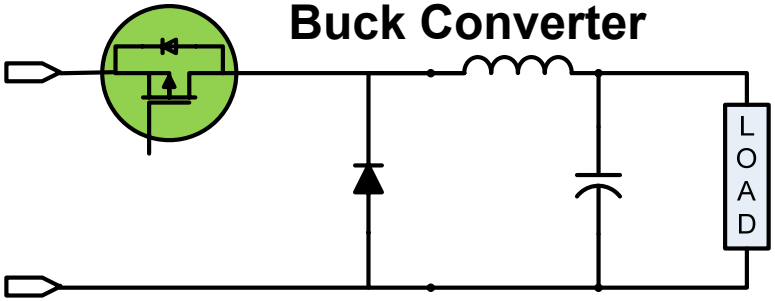
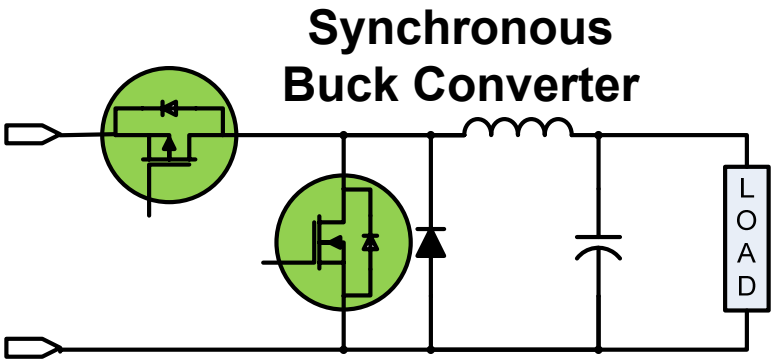
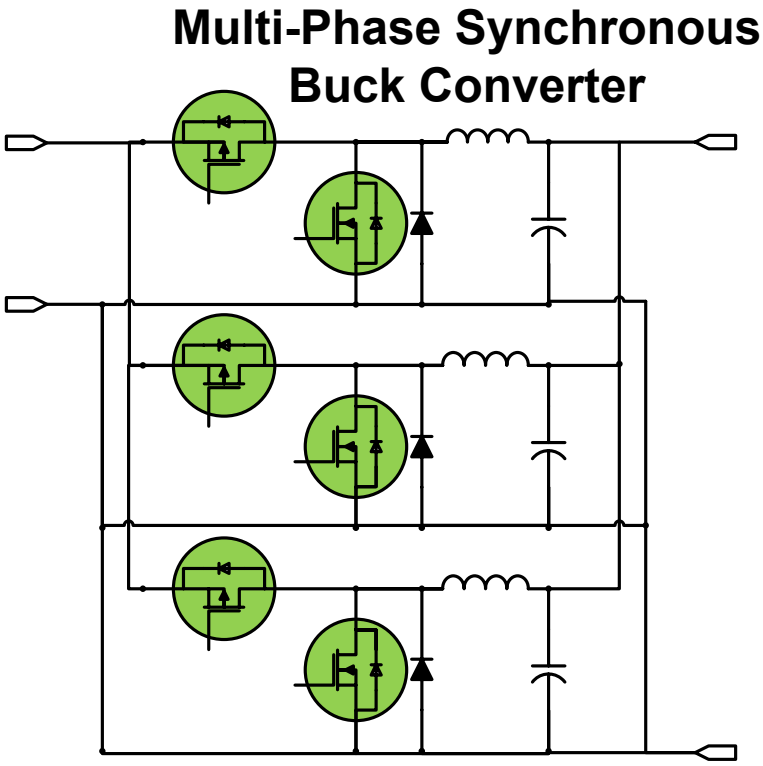
Output Stage Requirements







- **Output Design Specifications determine Choice of Converter Topology**

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Summary

- **Overview of AC/DC Reference Design**
  - Design Specifications
  - Features of dsPIC® DSC SMPS Family
- **AC/DC Reference Design Architecture**
  - Block Diagram
  - Rationale Behind Chosen Architecture

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Power Factor Correction

Additional Information Available in 11092_PFC

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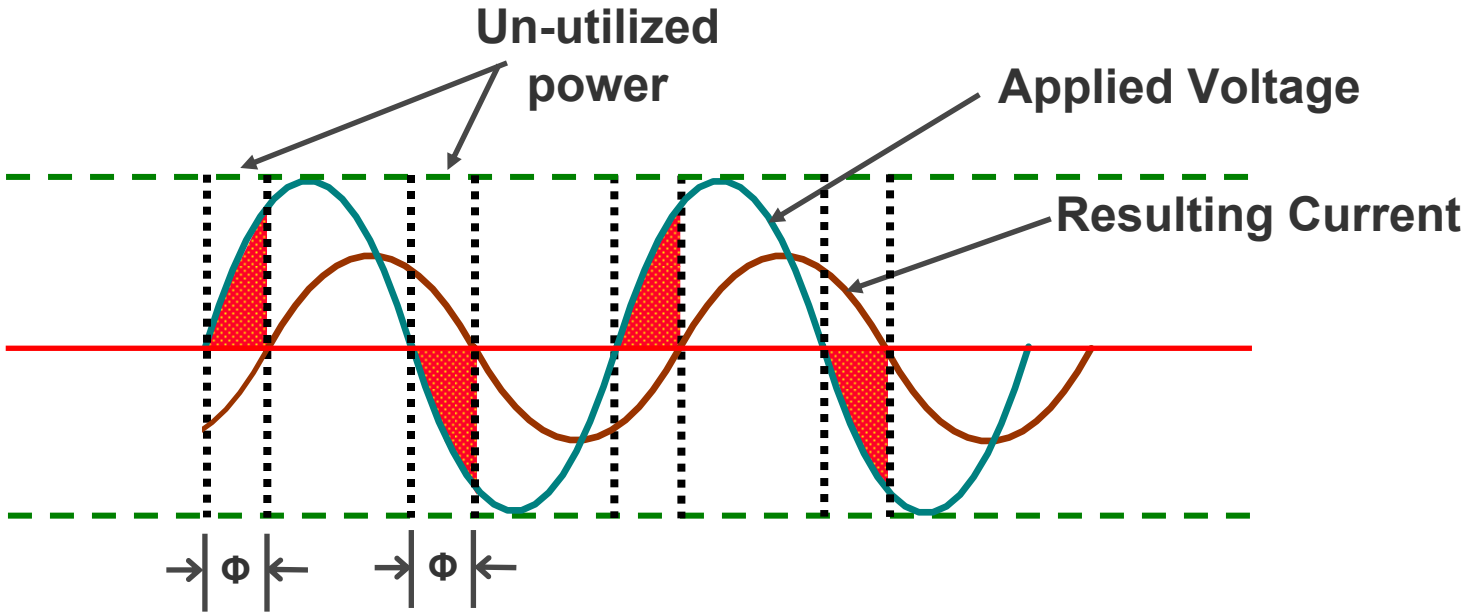
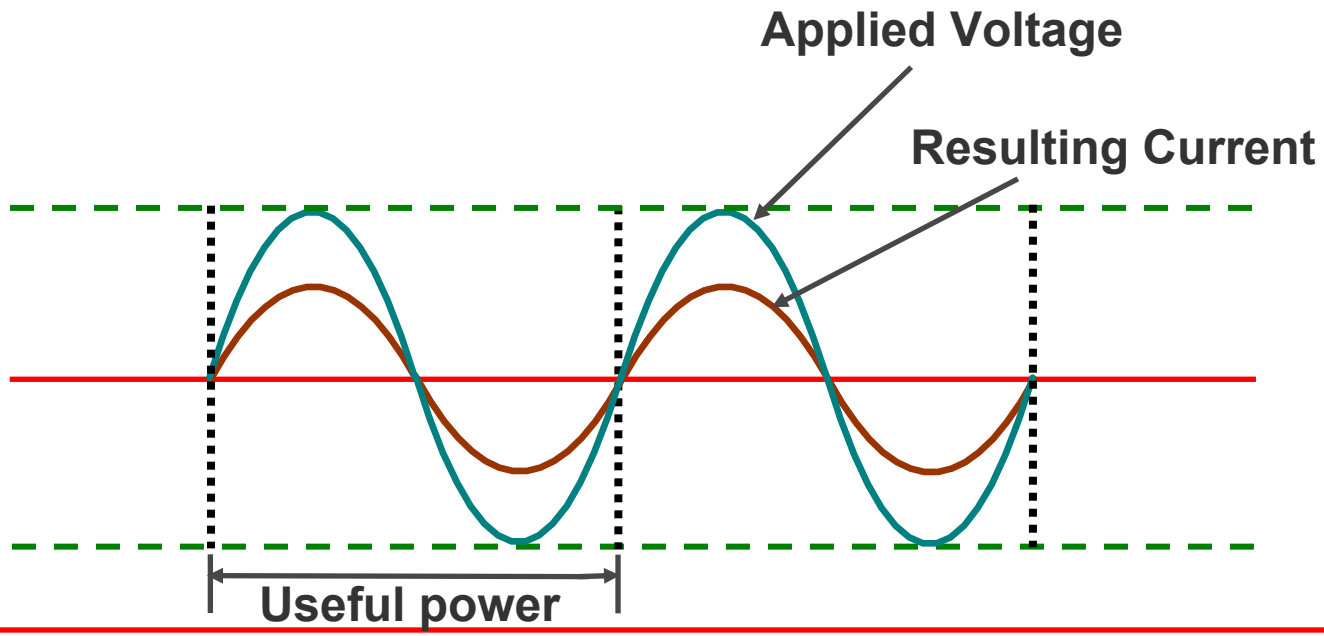
What is Power Factor ?





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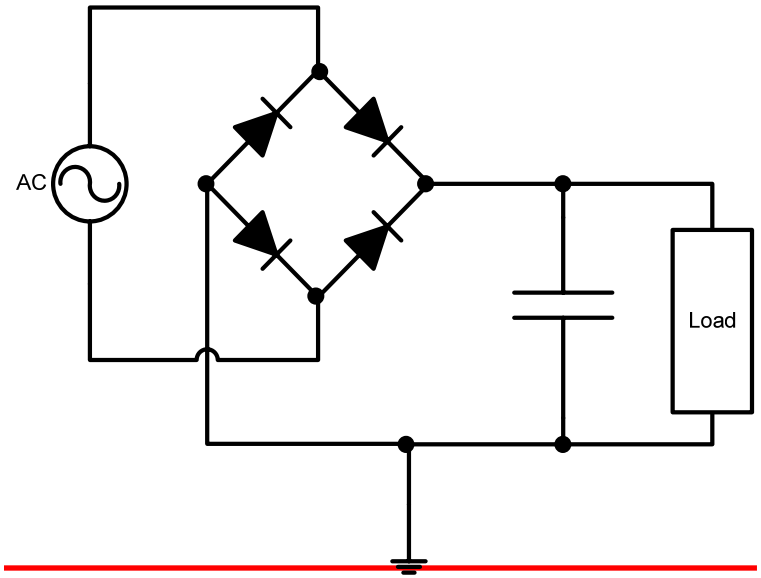
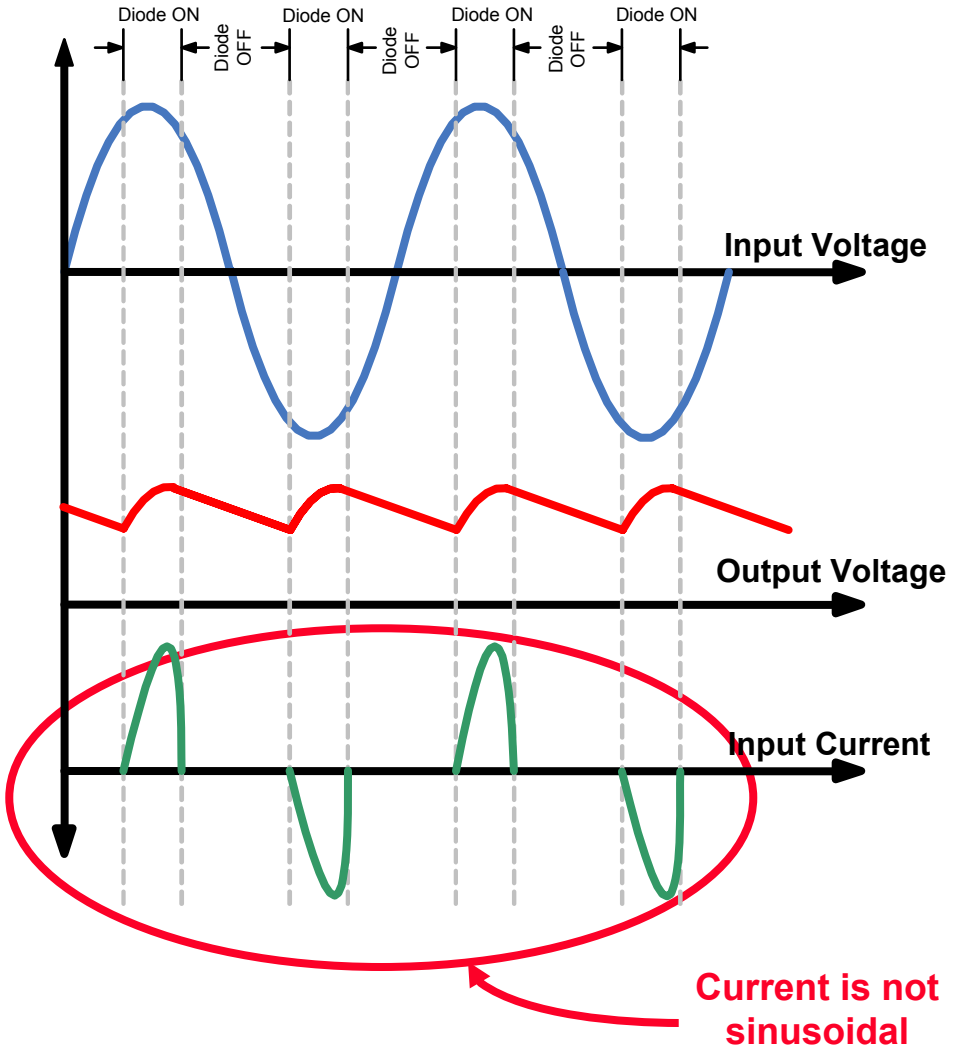
Power Factor Correction

- With no Power Factor Correction, the input current is highly distorted
- Induces Noise in the Power Grid
- Higher current rating device is required





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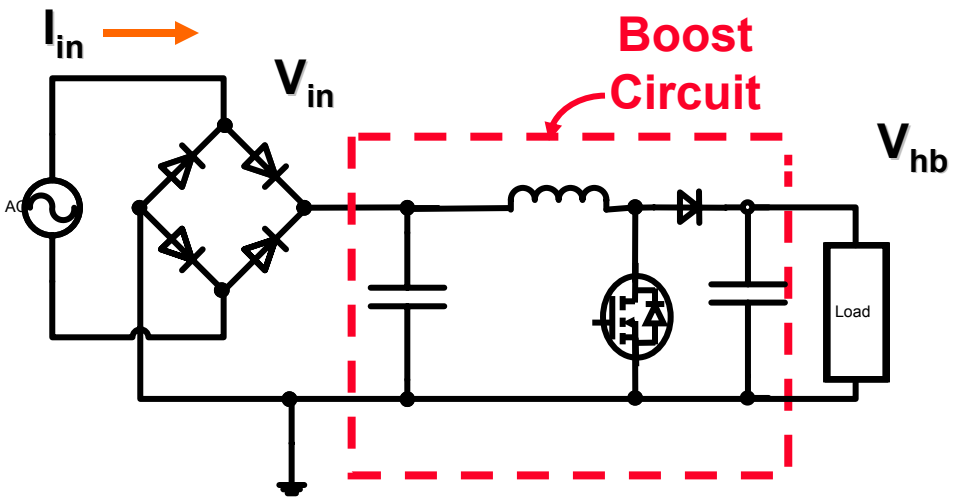
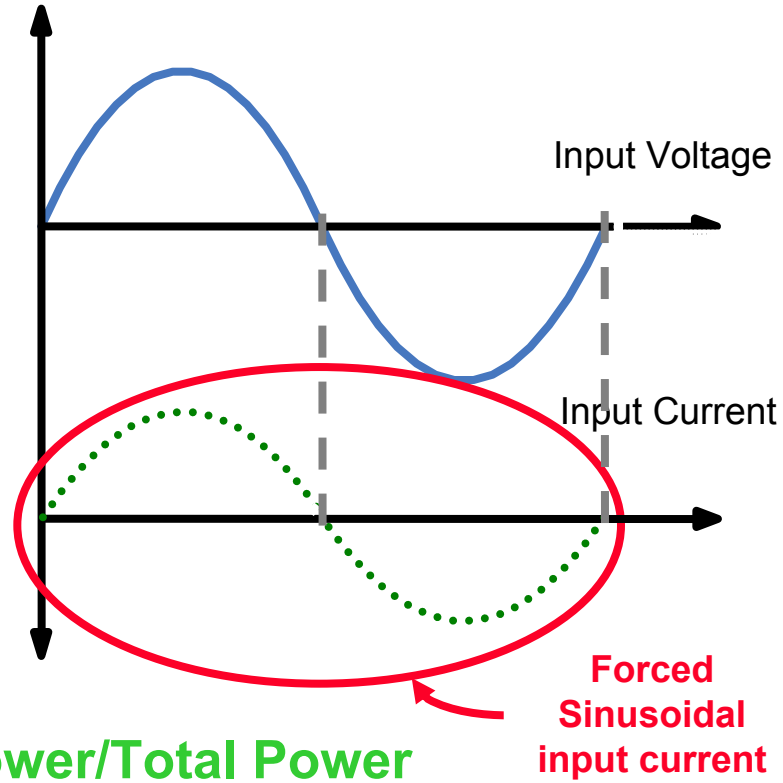
Power Factor Correction





- P.F. = Real (Active) component of Power/Total Power
- Need to sense Vin, Inductor Current and V_{hb}
- Maintains a Noise-free power grid
- Reduce rms and peak current required by the system

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Why is PFC needed?

- Reduce Peak Current Ratings
- Reduce Component Overheating
- Efficiently utilize available Power
- Comply with Regulations
- Avoid Penalties from Utility Company

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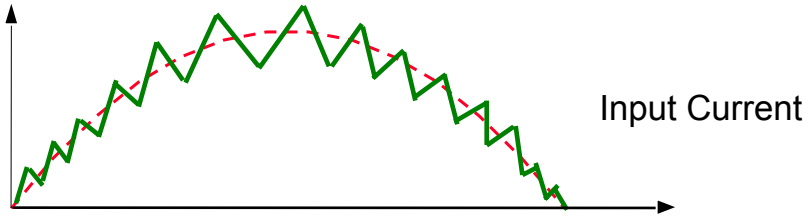
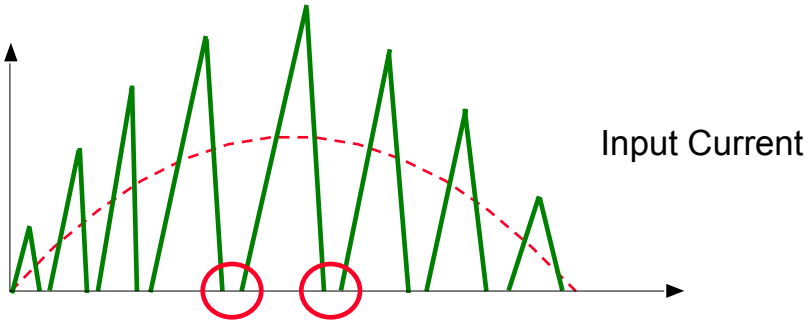
Common PFC Methods

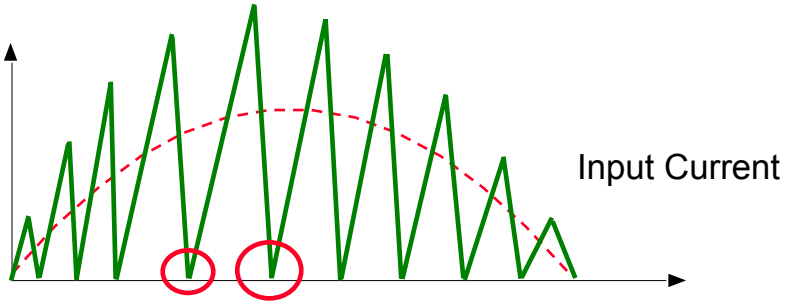
- Continuous Current Mode



- Discontinuous Current Mode



- Critical Conduction Current Mode



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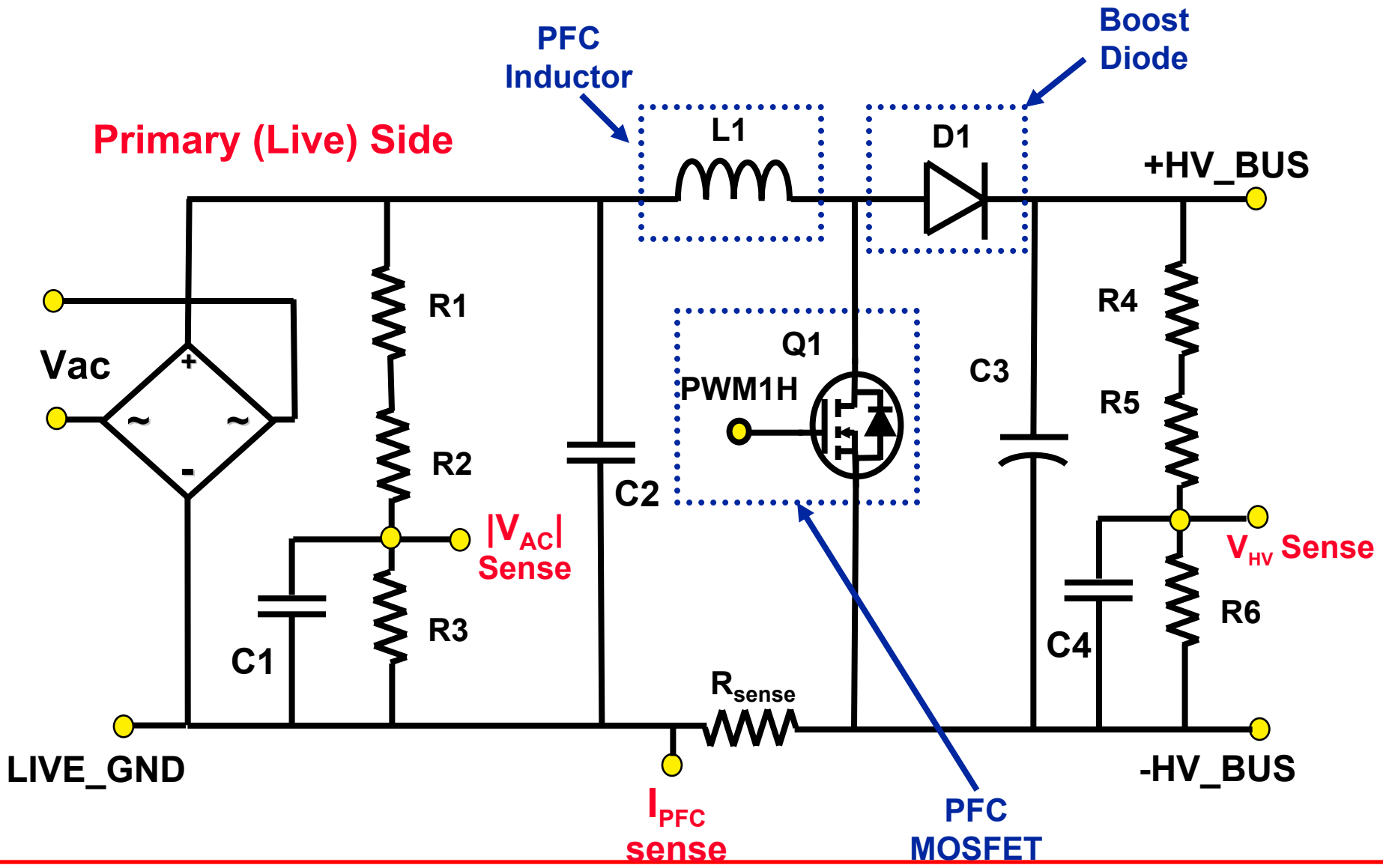
PFC Boost Converter



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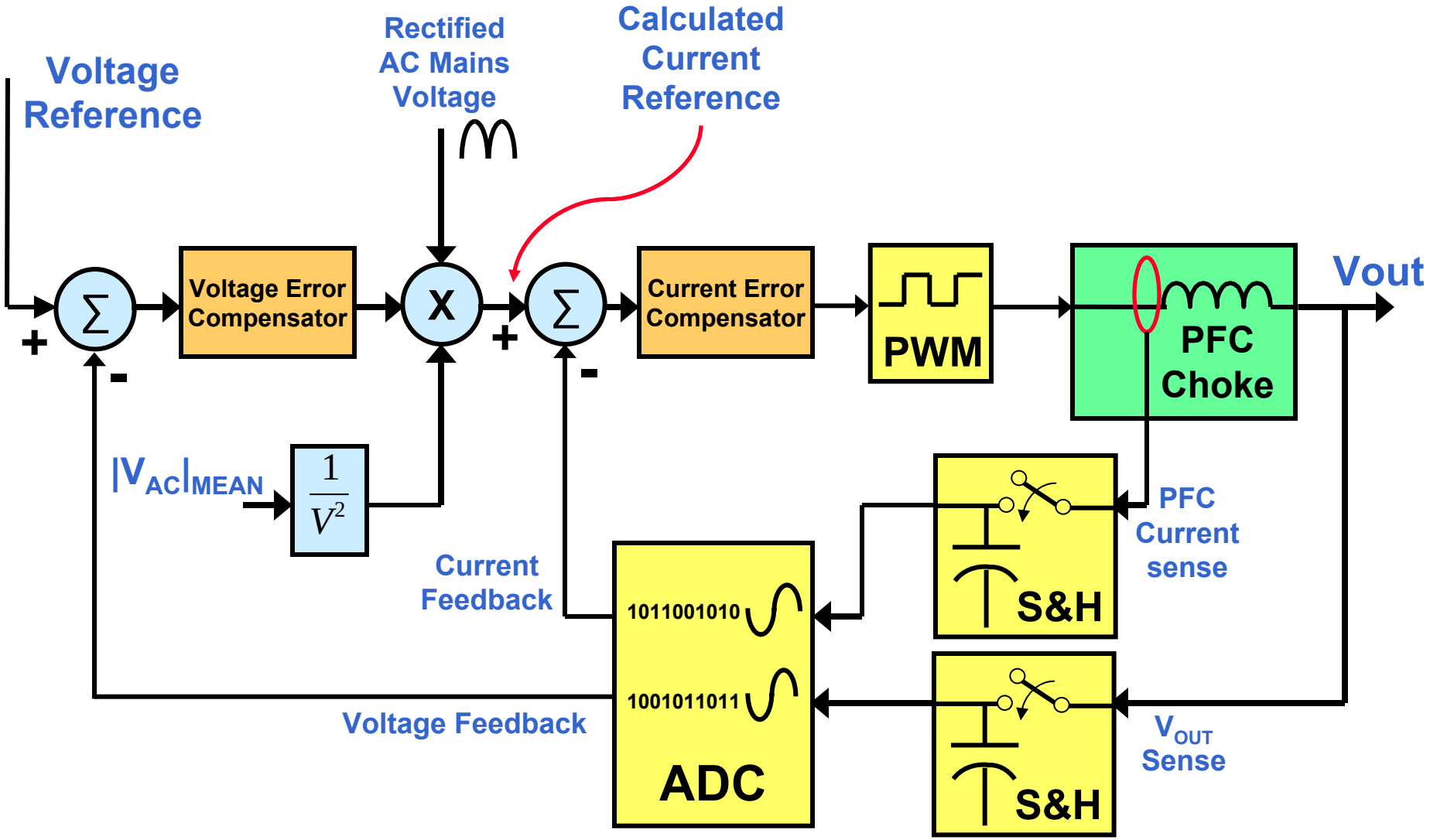
PFC Control Scheme



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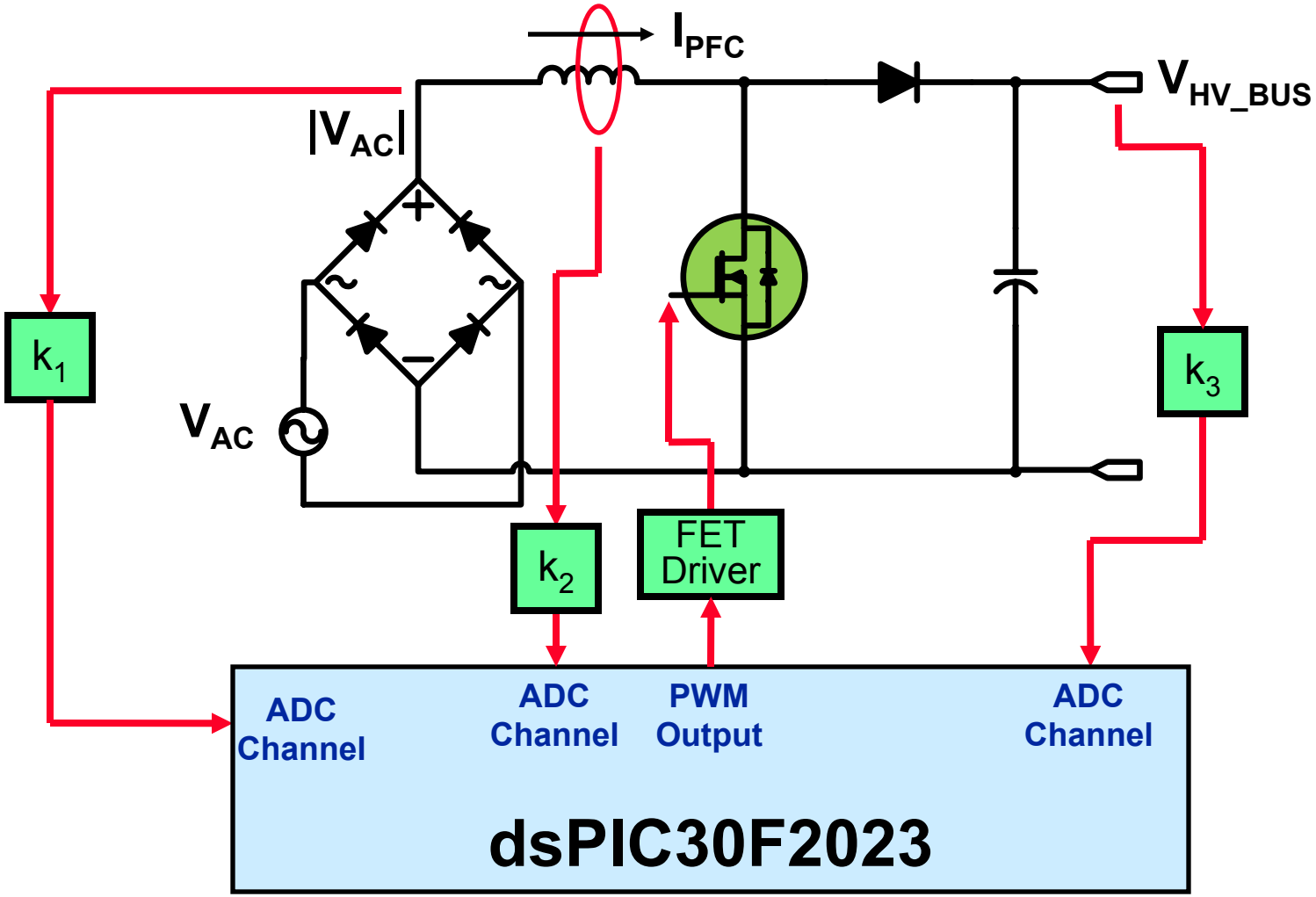
Resources Required for Digital PFC



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PFC Resource Allocation

Signal Name	Type of Signal	dsPIC® DSC Resource Used
V_{OUT}	Analog Input	AN5
I_{PFC}	Analog Input	AN4
$\|V_{AC}\|$	Analog Input	AN6
MOSFET Gate Drive	Drive Output	PWM4L
Current Loop Trigger	dsPIC® DSC Internal Signal	PWM4 Trigger to Sample PFC Current
Voltage Loop Trigger	dsPIC® DSC Internal Signal	Timer2

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PFC Control Software

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PFC Software Overview

- ADC Conversions are initiated by the PWM Trigger Feature
- The Current Control Loop is Executed in the ADC Interrupt Routine
- The Voltage Loop is Executed in a Timer Interrupt
- Faults are handled by the PWM Module using the on-chip Analog Comparators

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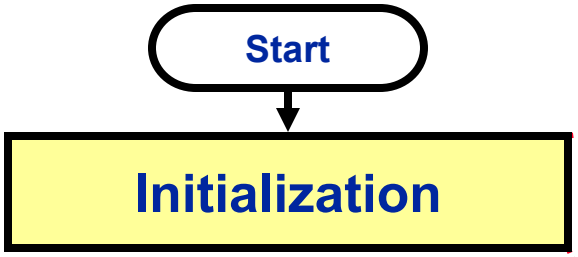
Structure of the PFC Software



- Initialize PWM
- Initialize ADC
- Setup Timer
- Configure Interrupts
- Initialize Control Loop Variables

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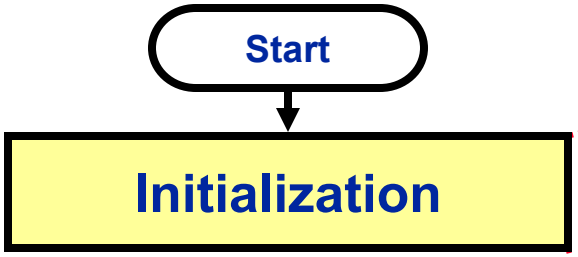
Structure of the PFC Software



- **Initialize PWM**
  - Configure PWM Mode, Output Polarity, Period, initial Duty Cycle
  - Setup PWM Faults and Fault Thresholds
  - Setup PWM Triggers

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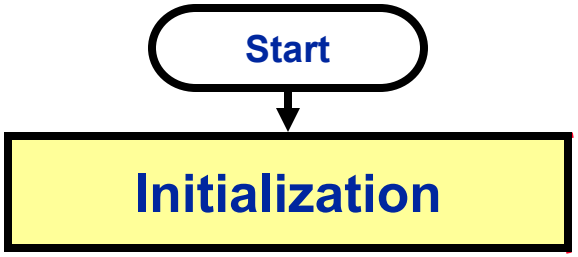
Structure of the PFC Software



- **Initialize ADC**
  - Setup ADC Speed
  - Configure desired ADC channels as analog inputs
  - Choose ADC Trigger Sources
  - Configure ADC Data Format
  - Choose Simultaneous or Sequential Sampling

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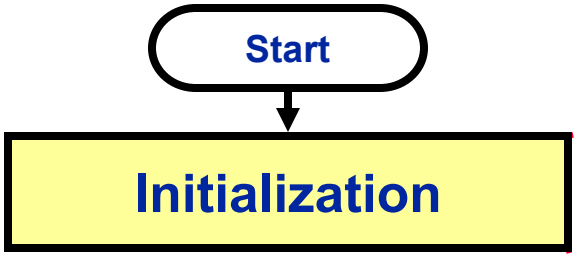
Structure of the PFC Software



- **Configure Timer**
  - Use Timer to trigger Voltage Control Loop
- **Setup Interrupts**
  - PWM Interrupt for Fault Handling
  - ADC Interrupt to trigger Current Control Loop
  - Timer Interrupt to trigger Voltage Control Loop

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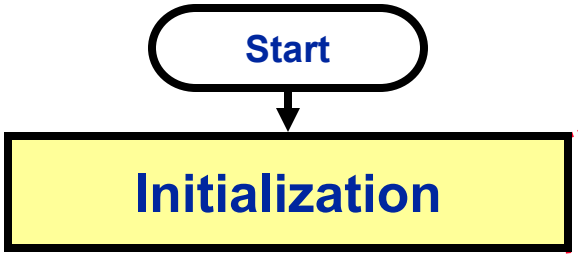
Structure of the PFC Software



- **Initialize Control Loop Variables**
  - Initialize PID Gain Terms in X-memory
  - Initialize Measured signals in Y-memory
  - Initialize pointers to Control Loop Inputs and Outputs

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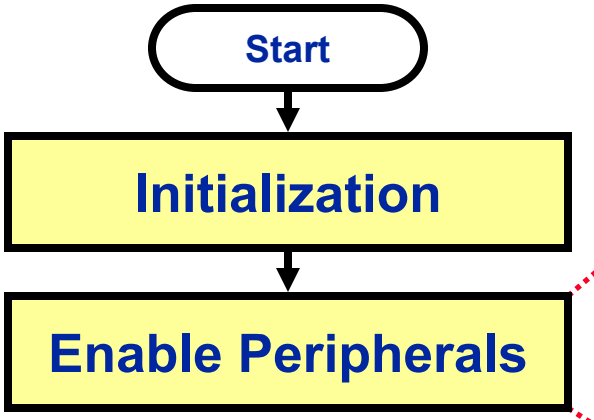
Structure of the PFC Software



- **Enable Peripherals**
  - Enable Timer
  - Enable ADC
  - Enable PWM

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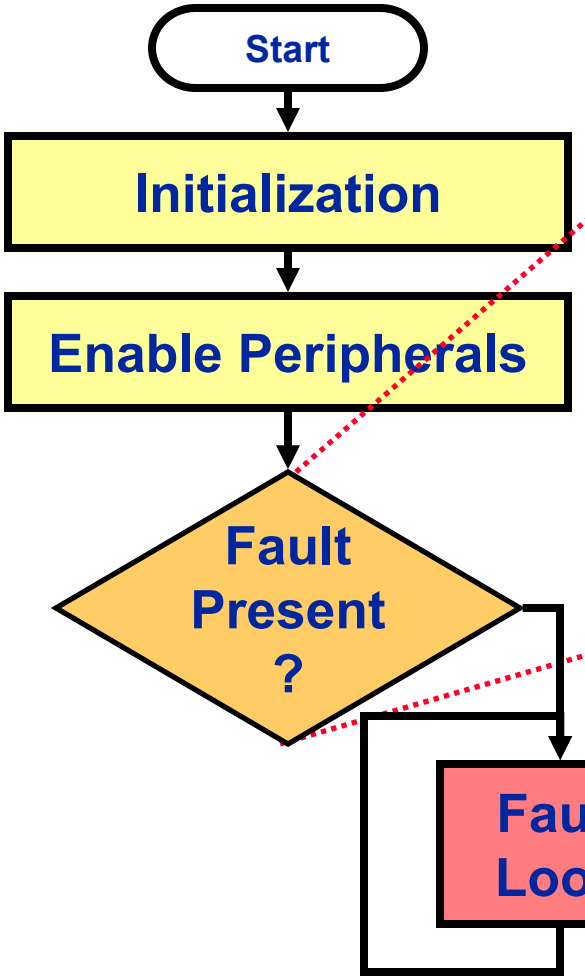
Structure of the PFC Software



- **Check for Faults**
  - The PWM Module is setup to detect Faults and Shutdown all Outputs
  - The PWM Fault Interrupt sets the Fault Flag
  - The Main Routine Checks the Fault Flag

- **Fault Loop**
  - The Fault Indicator LED is enabled
  - Any other Fault Handling Routines can be placed in this loop

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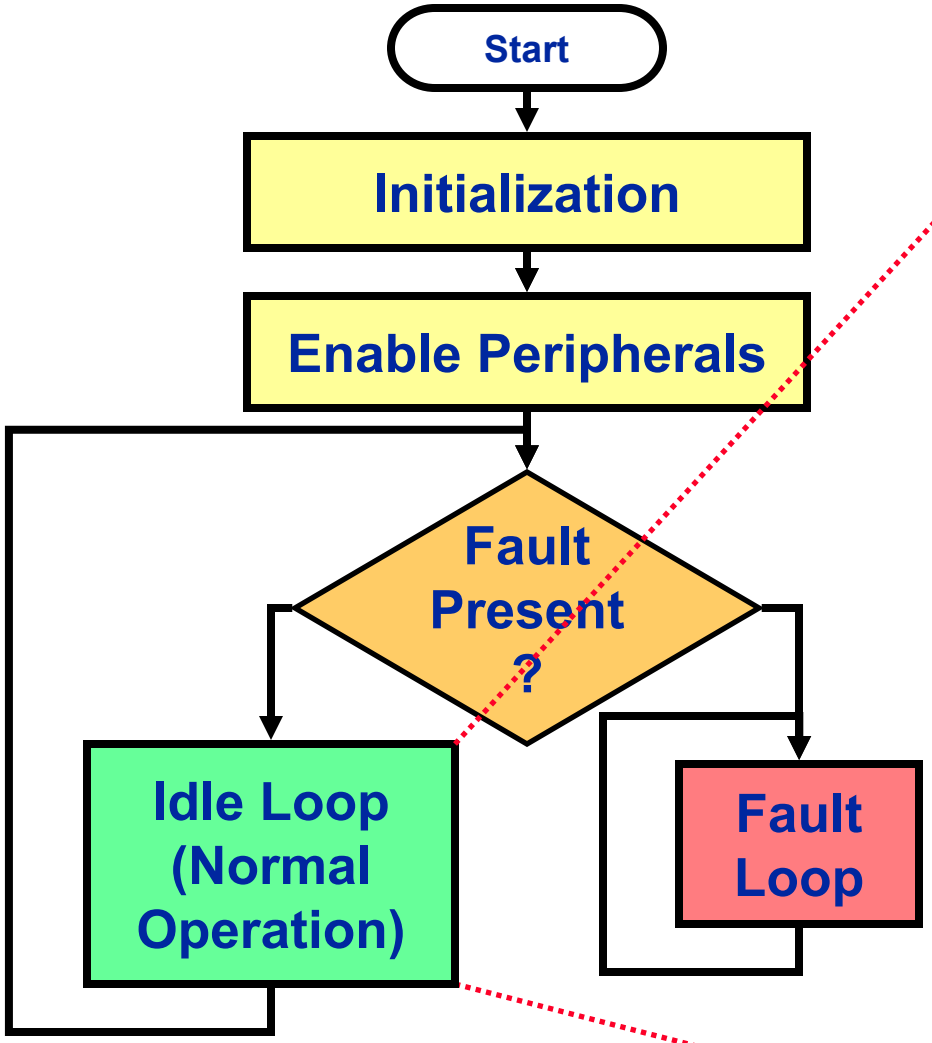
Structure of the PFC Software



- **Idle Loop (Low Priority)**
  - Input AC Voltage Measurement
  - Power Management Routines
  - Check Temperature
  - Other Auxiliary Features

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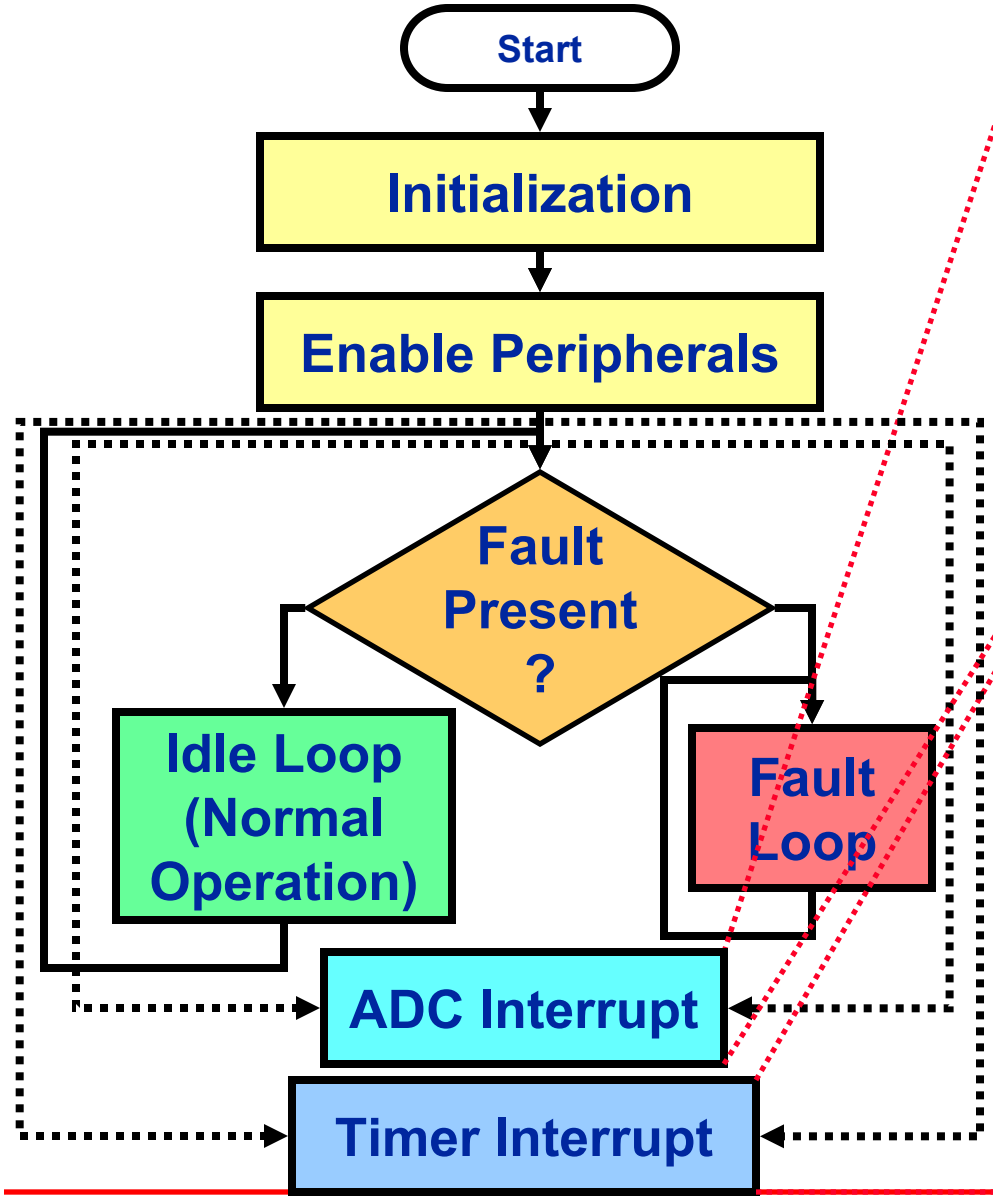
Structure of the PFC Software



- **ADC Interrupt (High Priority)**
  - PFC Current Loop
    - **PFC Current Measurement**
    - **Current PID Calculations**
    - **Update PWM Duty Cycle**

- **Timer Interrupt (Medium Priority)**
  - PFC Voltage Loop
    - **V_{OUT} Measurement**
    - **Voltage PID Calculations**
    - **Update PFC Current Reference**

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Demonstration #1

Digital Power Factor Correction

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Zero Voltage and Zero Current Switching

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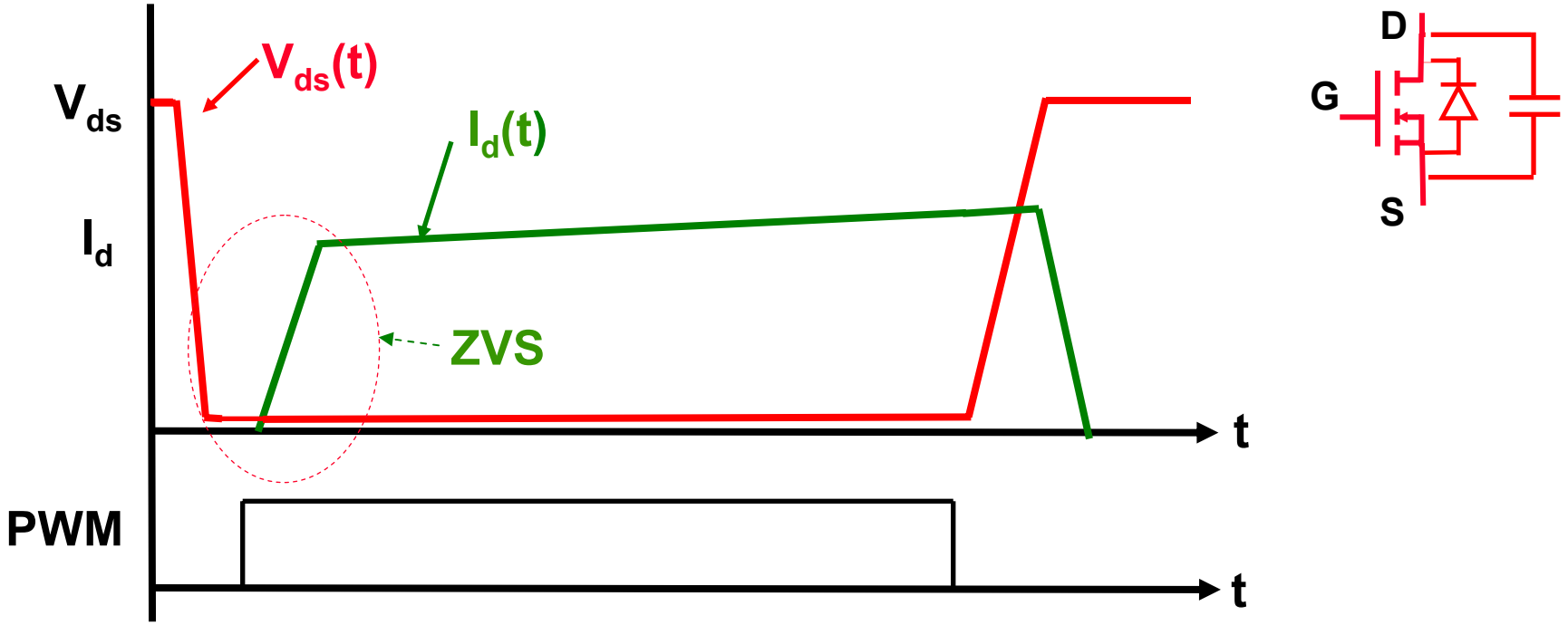
Zero Voltage Switching

- At transition period from one state to another state of the switch, the voltage is zero, hence no losses



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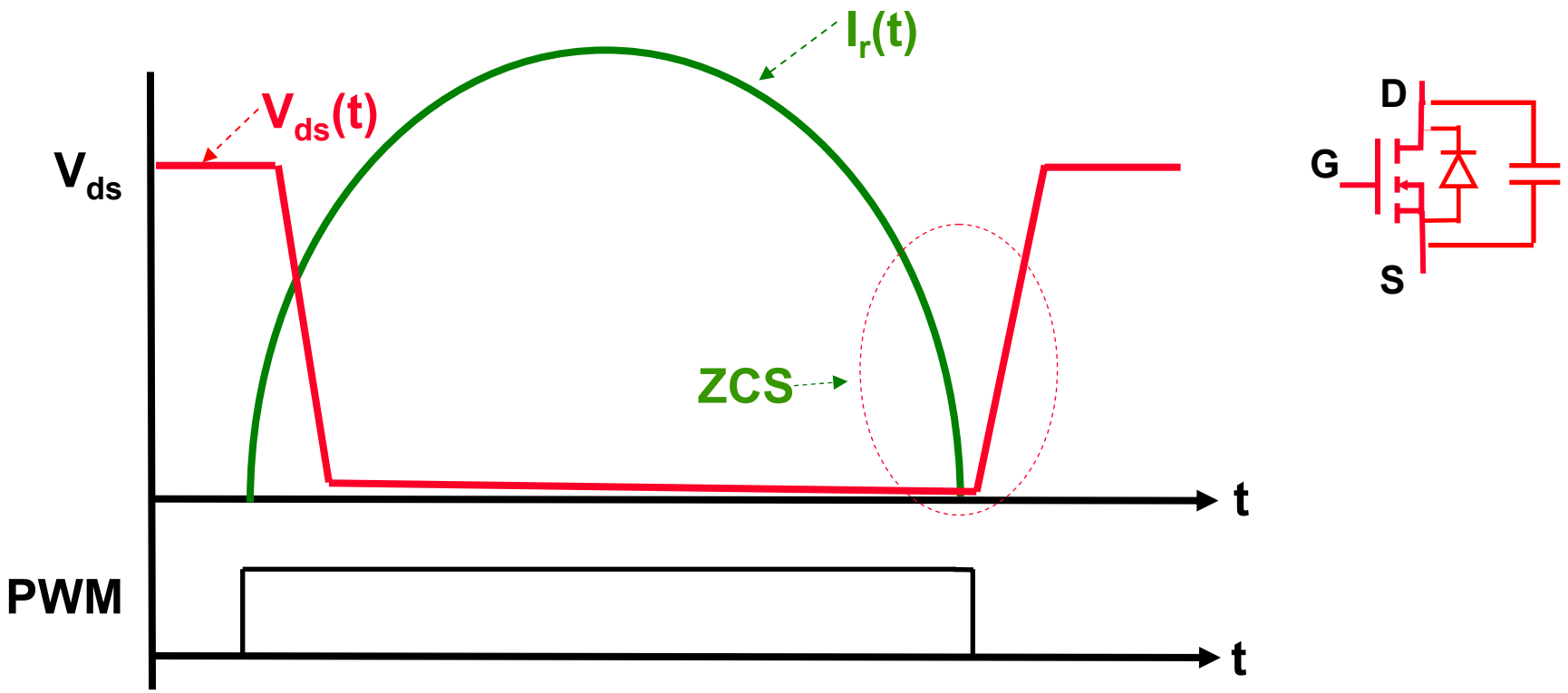
Zero Current Switching

- At transition period from one state to another state of the switch, current is zero, hence no losses



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Switching Methodology

- **Zero Current Switching:**
  - Eliminates V*I losses in switching device during transitions
  - Reduces Noise in the system hence better EMI performance
  - Can be implemented at switch Turn ON as well as Turn OFF
  - RMS Current through switch increases and therefore higher conduction losses

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Switching Methodology

- **Zero Voltage Switching :**
  - Eliminates V*I losses in switching device during transitions
  - Reduces Noise in the system hence better EMI performance
  - Eliminates MOSFET output capacitor (C_{oss}) loss during switch Turn-ON
  - Preferred in high voltage high power system

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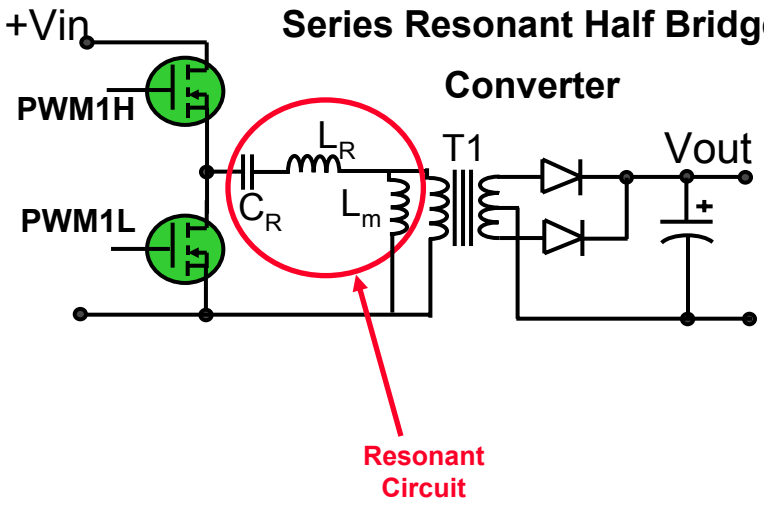
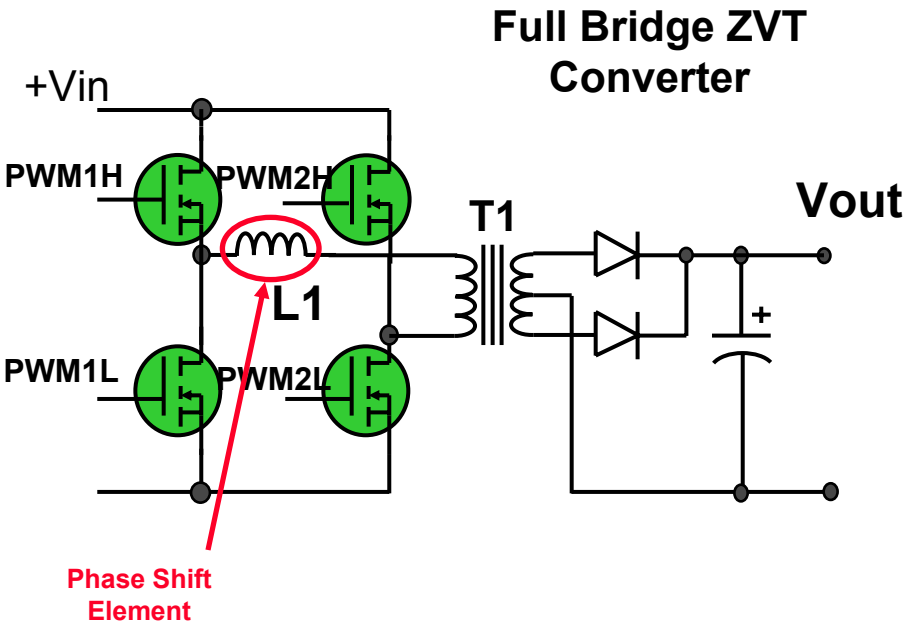
Soft Switching Topologies

- **Resonant Mode**
  - SRC – Series Resonant
  - PRC – Parallel Resonant
  - LLC Resonant
- **Zero Transition**
  - ZVT – Zero Voltage Transition





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Full-Bridge ZVT Converter

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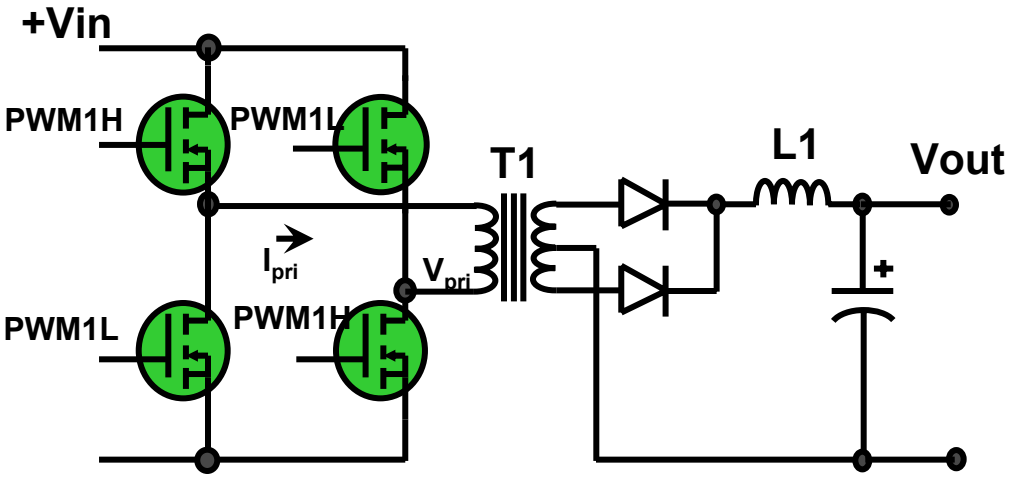
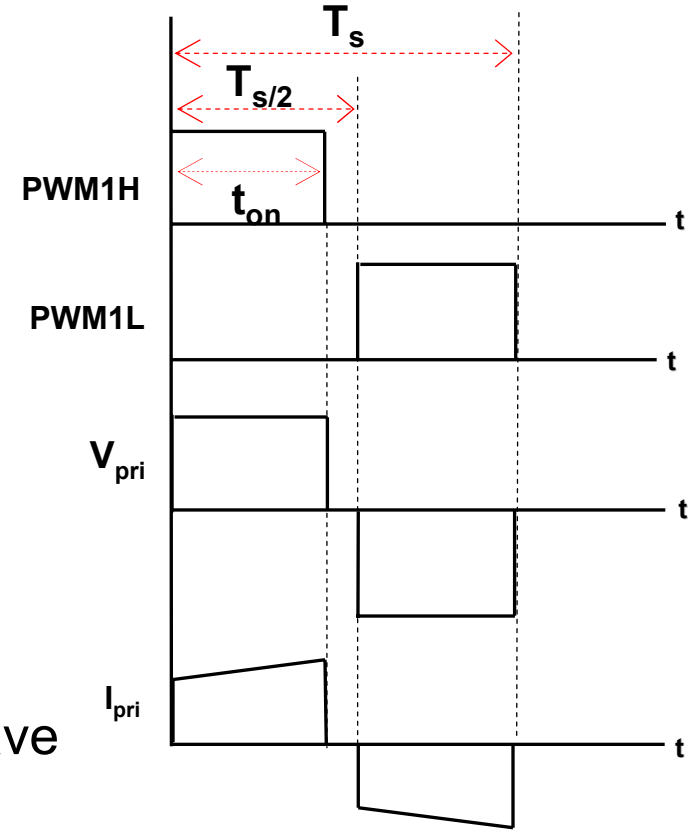
Full-Bridge Converter





- **Full bridge converter**
  - Buck derived isolated converter
  - Push Pull mode of PWM gate pulses
  - Each half-bridge produces square wave voltage
  - Duty cycle ratio controls the power flow
  - Turn ON as well as Turn OFF losses in the MOSFET
  - Popular for high power application

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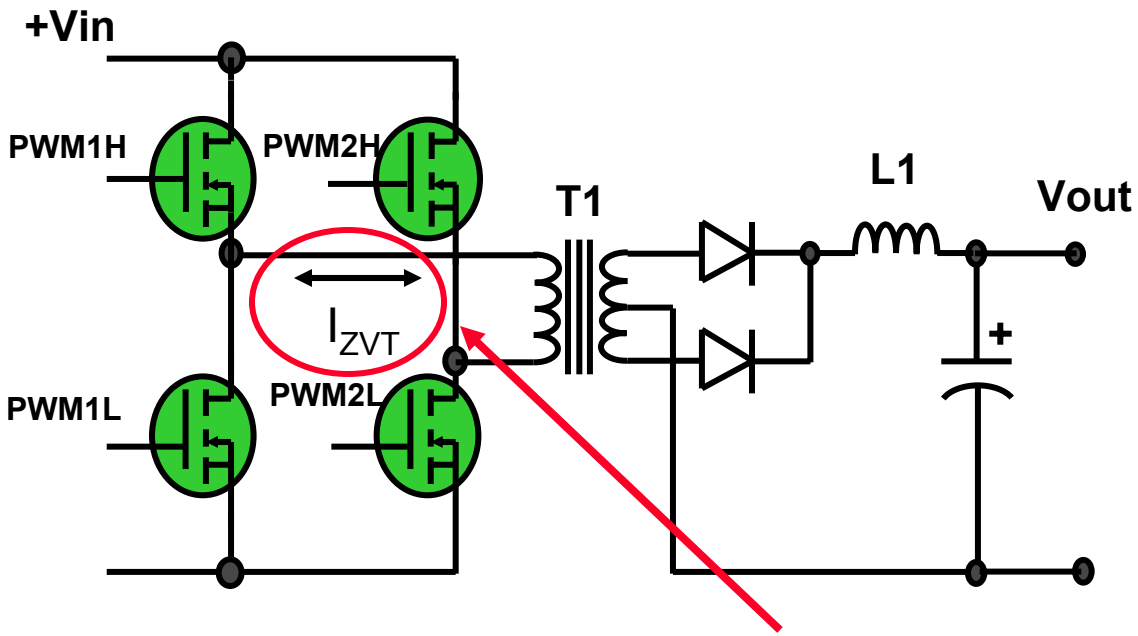
Flux Walking



- Flux Walking – small DC magnetic offsets add up over time to create magnetic saturation
- Flux Walking can be prevented by monitoring the current in both directions and making corrections if necessary

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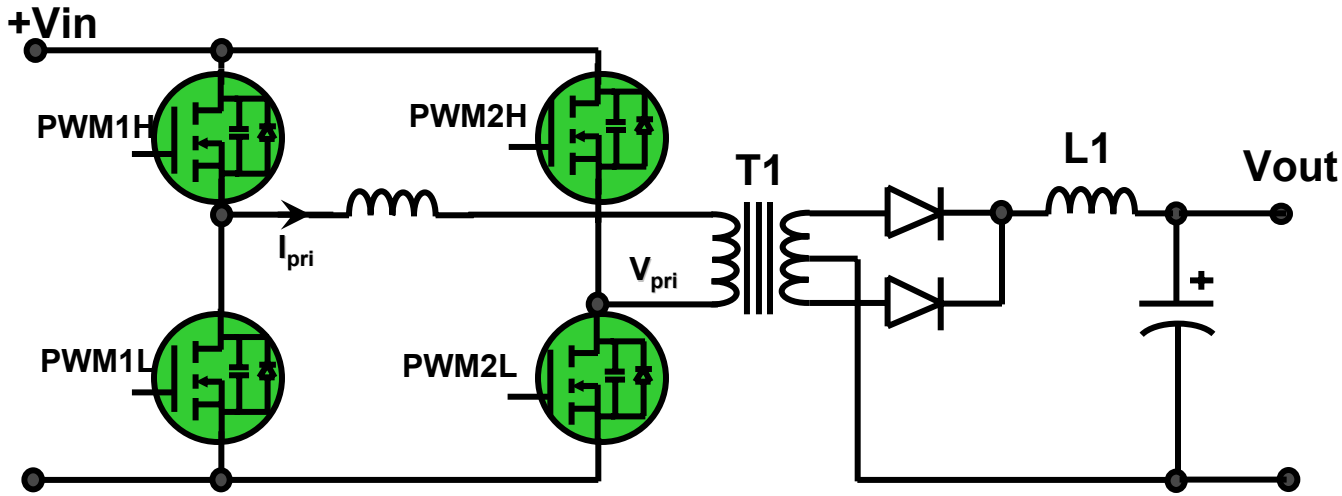
Full-Bridge Phase Shift ZVT Converter



- **Full-bridge Phase Shift ZVT converter**
  - Complementary, fixed duty cycle PWM gate pulses
  - Phase shift in gate pulse of two legs control the power flow
  - Zero Voltage Switching, hence Turn ON losses in the MOSFET eliminates
  - Parasitic of MOSFET and Transformer used to achieved ZVT
  - A popular converter for very high power application

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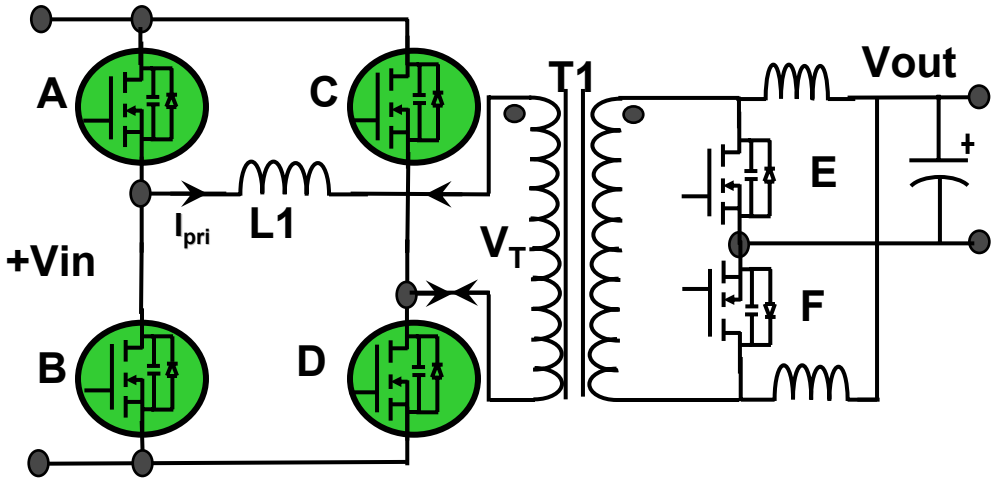
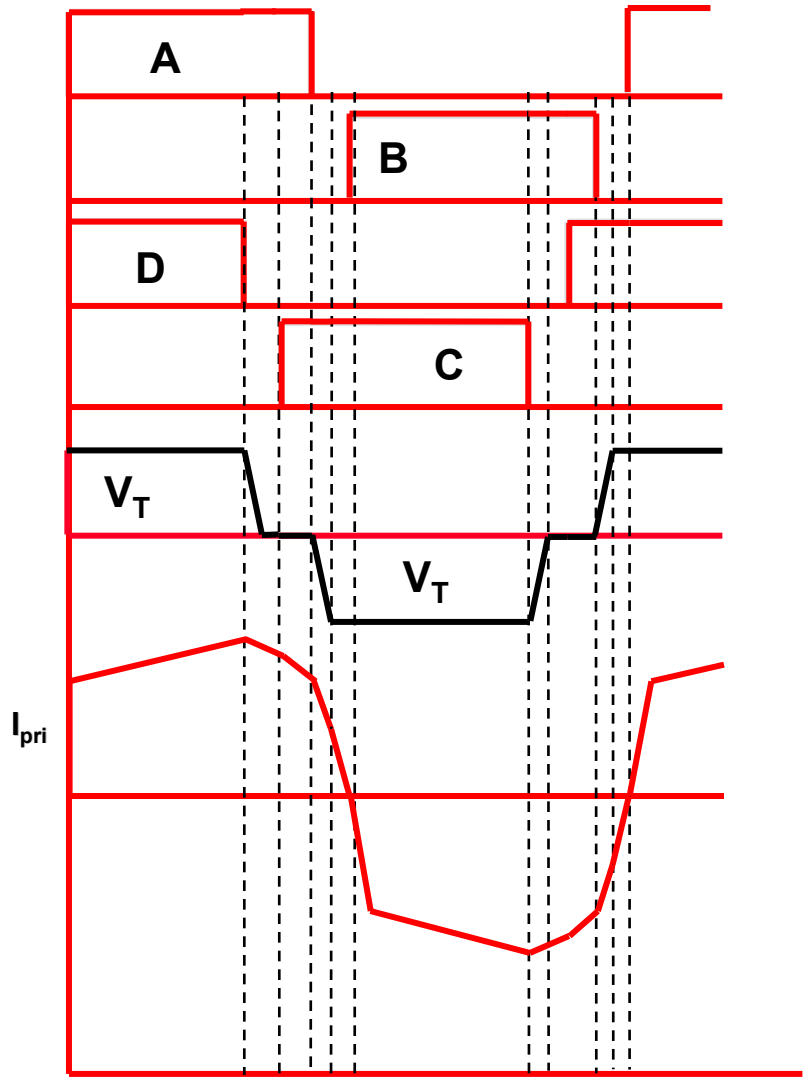
Full-Bridge Phase Shift ZVT Converter





- **Right leg transition**
  - Terminates the power delivery interval
  - Reflected load current is driving ZVS
  - Transition is linear
  - End of this period transformer primary is short circuited
- **Left leg transition**
  - Begins after freewheeling state to initiate the power delivery
  - Energy stored in the inductor drives the ZVS
  - Transition is resonant and non linear

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Full-Bridge Phase Shift ZVT Converter

- The right leg transition period is given by:
  - Time required to charge and discharge the output capacitor of MOSFET C and MOSFET D

$$dt = C_r \cdot \frac{dv}{I_p}$$

- The left leg transition period is given by:
  - Resonant time between L1 and output capacitor of MOSFET (A+B)

$$dt = \frac{\pi}{2} \cdot \sqrt{L1 \cdot C_r}$$

Where, dt = transition time

I_p = primary current when the MOSFET D turns OFF

L1 = Leakage inductance of transformer

C_r = equivalent capacitor of MOSFET two MOSFET and transformer parasitic capacitor (C_{xfmr})

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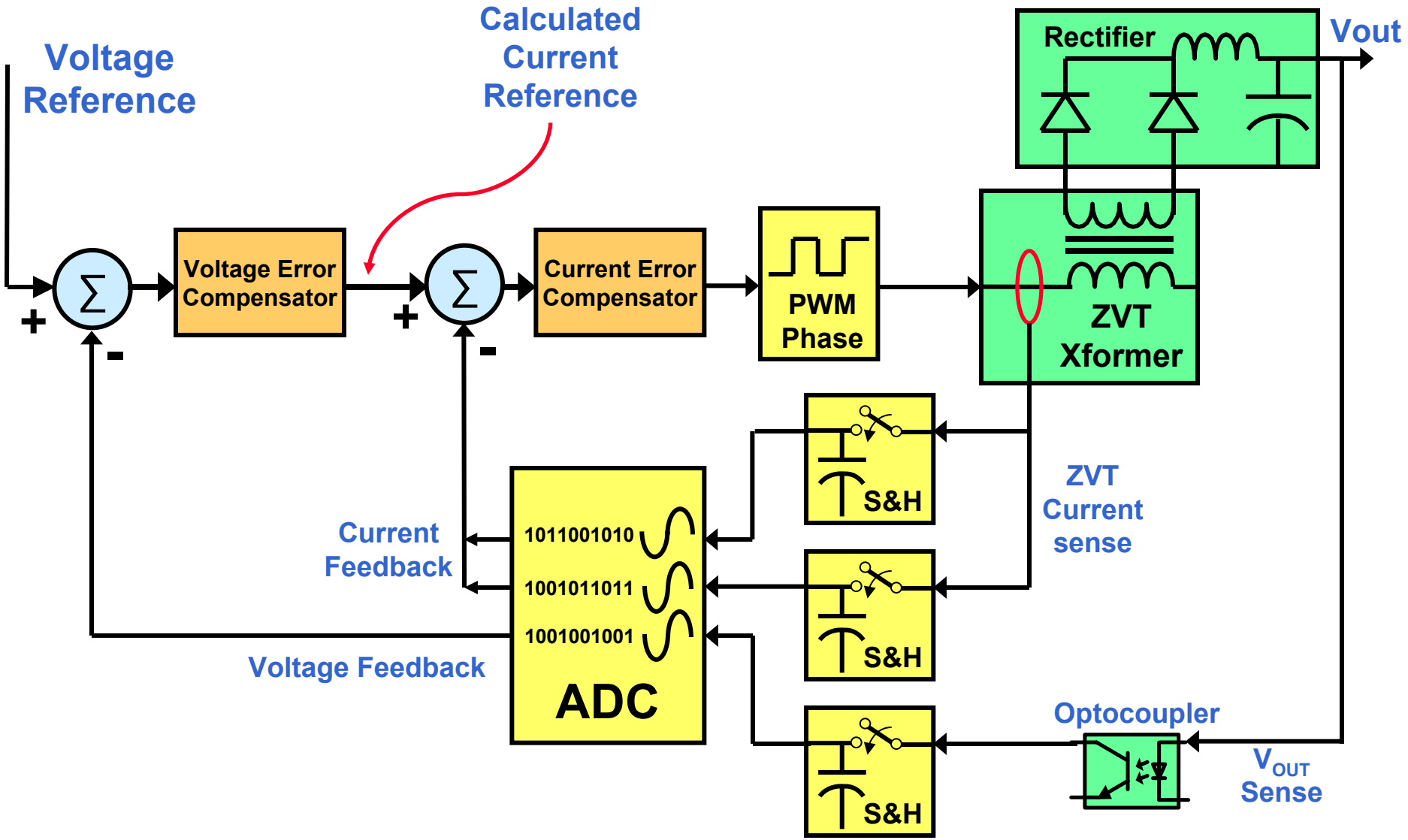
ZVT Control Scheme



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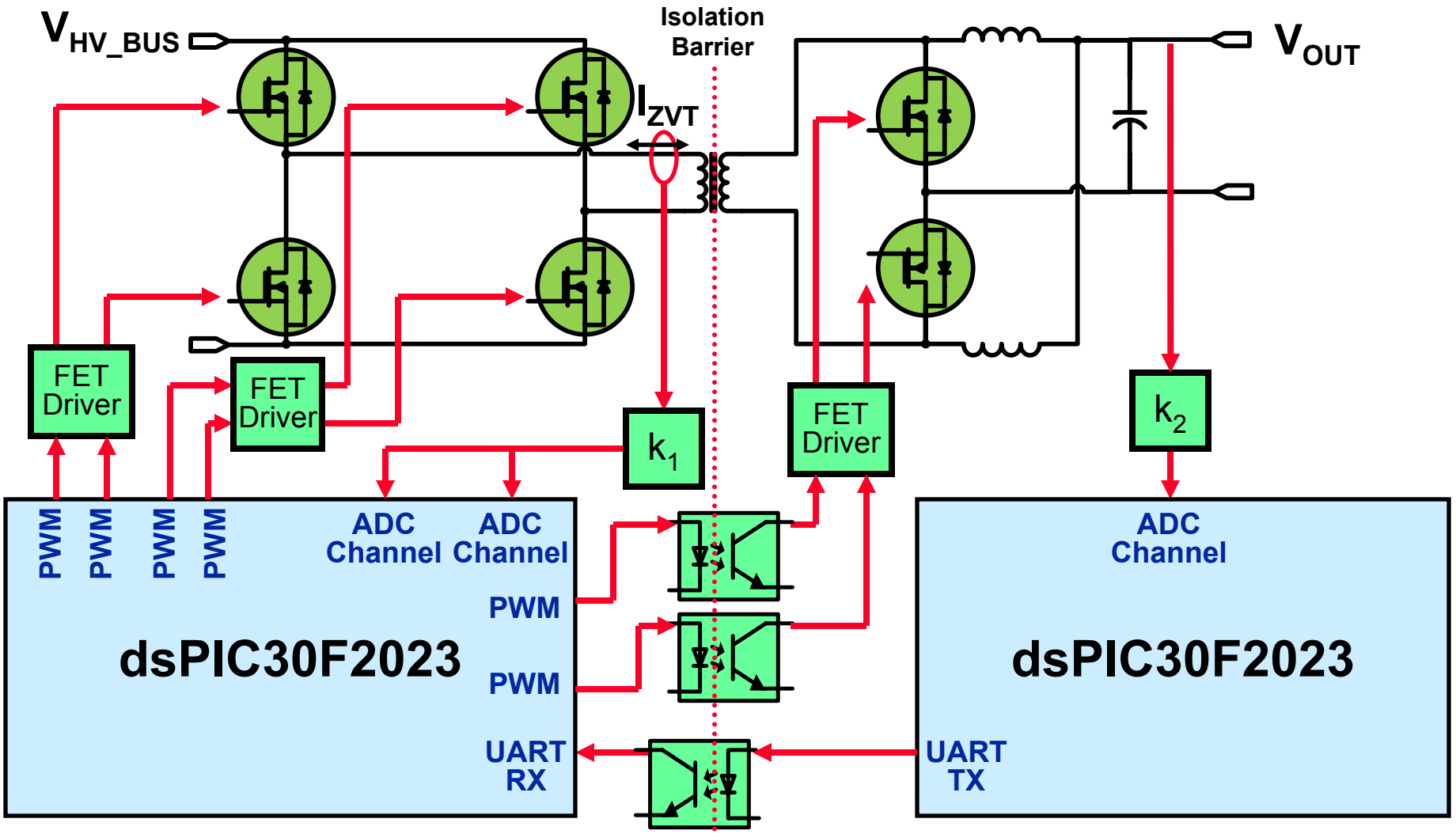
Resources Required for Digital ZVT Converter



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ZVT Resource Allocation

Signal Name	Type of Signal	dsPIC® DSC Resource Used
I_{ZVT1}	Analog Input	AN0
I_{ZVT2}	Analog Input	AN2
V_{OUT}	UART Input	U1RX
ZVT Gate Drive	Drive Outputs	PWM1H, PWM1L PWM2H, PWM2L
Sync. Rectifier Gate Drive	Drive Outputs	PWM3H, PWM3L
Current Loop Trigger	dsPIC® DSC Internal Signal	PWM1, PWM2 Triggers to Sample ZVT Current
Voltage Loop Trigger	dsPIC® DSC Internal Signal	UART1

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Agenda

- **Overview of AC/DC Reference Design**
- **AC/DC Reference Design Architecture**
- **Power Factor Correction**
  - PFC Control Software
- **Zero Voltage Transition**
  - ZVT Control Software
- **Multi-phase Buck Converters**
  - Multi-phase Buck Control Software
- **Enhanced Features**

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ZVT Control Software

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ZVT Software Overview

- ADC Conversions are initiated by the PWM Trigger Feature
- The Current Control Loop is Executed in the ADC Interrupt Routine
  - Additional Check for Transformer Primary Current Balance to prevent Flux Walking
- The Voltage Loop is Executed from a UART Receive Interrupt
- Faults are handled by the PWM Module using the on-chip Analog Comparators

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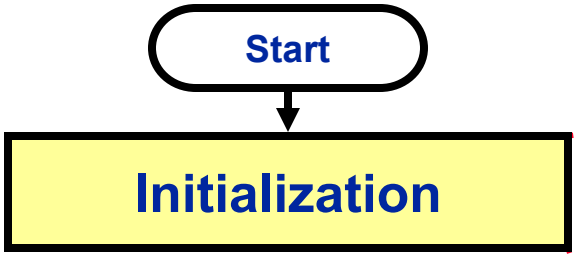
Structure of the ZVT Software



- Initialize PWM
- Initialize ADC
- Setup Timers
- Setup UART
- Configure Interrupts
- Initialize Control Loop Variables

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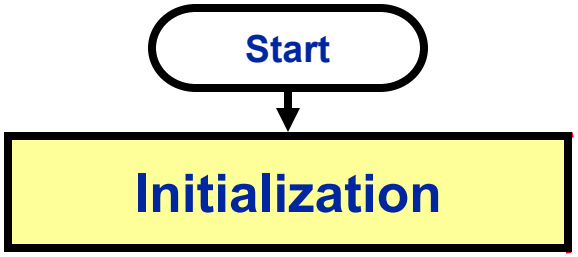
Structure of the ZVT Software



- **Initialize PWM**
  - Configure PWM Mode, Output Polarity, Period, Duty Cycle and Phase Shift
  - Setup PWM Faults and Fault Thresholds
  - Setup PWM Triggers

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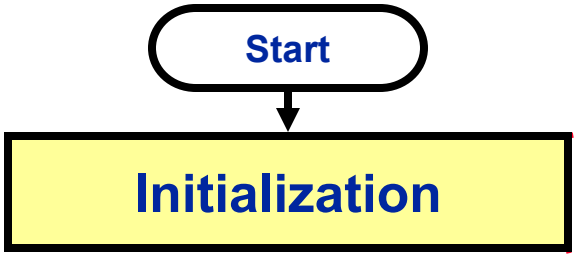
Structure of the ZVT Software



- **Initialize ADC**
  - Setup ADC Speed
  - Configure desired ADC channels as analog inputs
  - Choose ADC Trigger Sources
  - Configure ADC Data Format
  - Choose Simultaneous or Sequential Sampling

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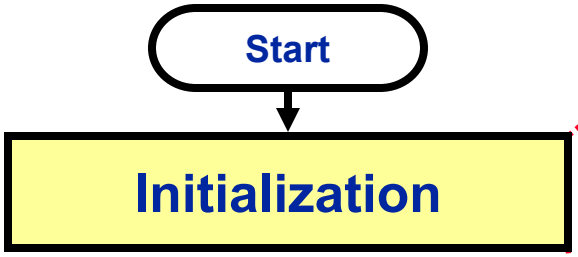
Structure of the ZVT Software



- **Configure Timers**
  - Use Timer to trigger Voltage Control Loop
- **Configure UART**
  - Use UART to receive V_{OUT} feedback signal
- **Setup Interrupts**
  - PWM Interrupt for Fault Handling
  - Timer Interrupt to trigger Voltage Control Loop
  - ADC Interrupt to trigger Current Control Loop
  - UART Receive Interrupt to Execute the Voltage Loop

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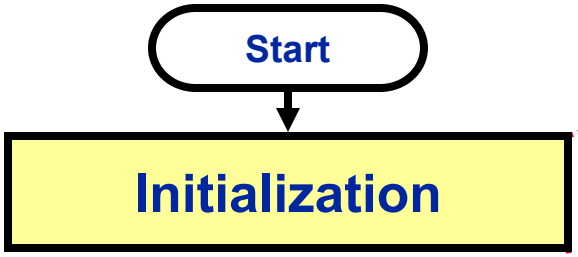
Structure of the ZVT Software



- **Initialize Control Loop Variables**
  - Initialize PID Gain Terms in X-memory
  - Initialize Measured signals in Y-memory
  - Initialize pointers to Control Loop Inputs and Outputs

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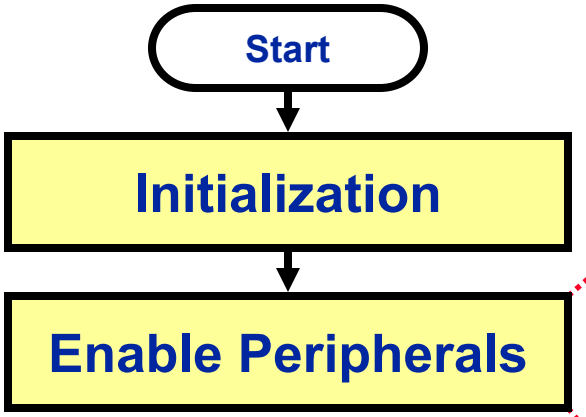
Structure of the ZVT Software



- **Enable Peripherals**
  - Enable Timers
  - Enable UART
  - Enable ADC
  - Enable PWM

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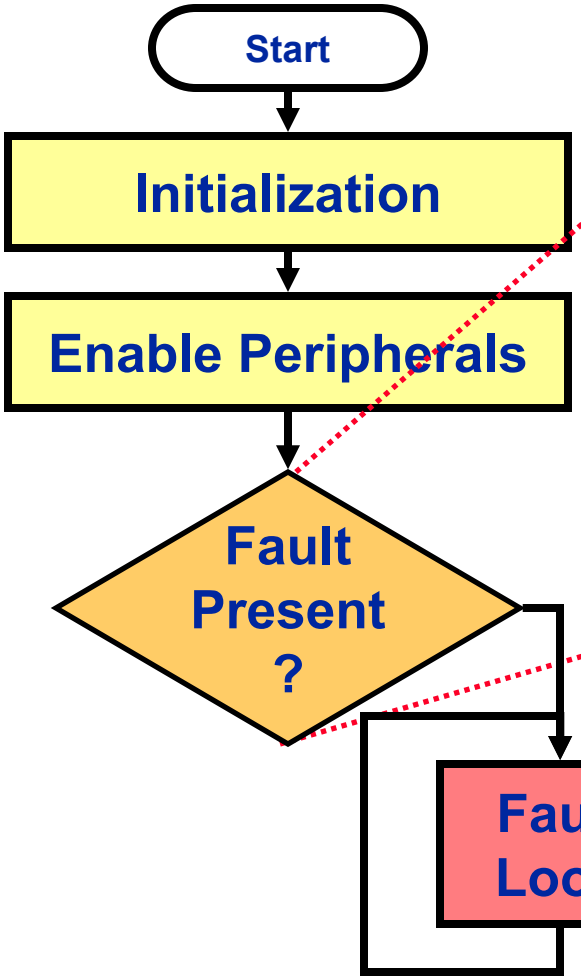
Structure of the ZVT Software



- **Check for Faults**
  - The PWM Module is setup to detect Faults and Shutdown all Outputs
  - The PWM Fault Interrupt sets the Fault Flag
  - The Main Routine Checks the Fault Flag

- **Fault Loop**
  - The Fault Indicator LED is enabled
  - Any other Fault Handling Routines can be placed in this loop

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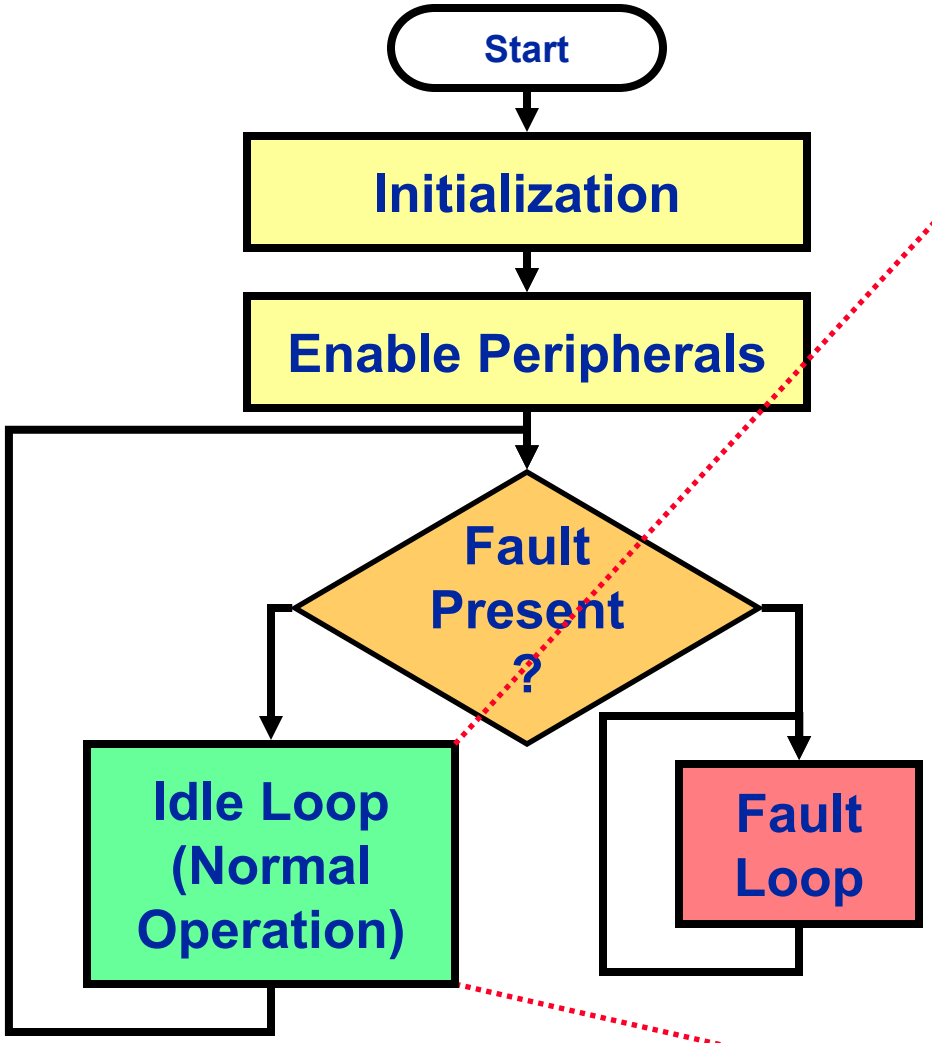
Structure of the ZVT Software



- **Idle Loop (Low Priority)**
  - Check Input Voltage
  - Check Temperature
  - Power Management Routines
  - Other Auxiliary Features

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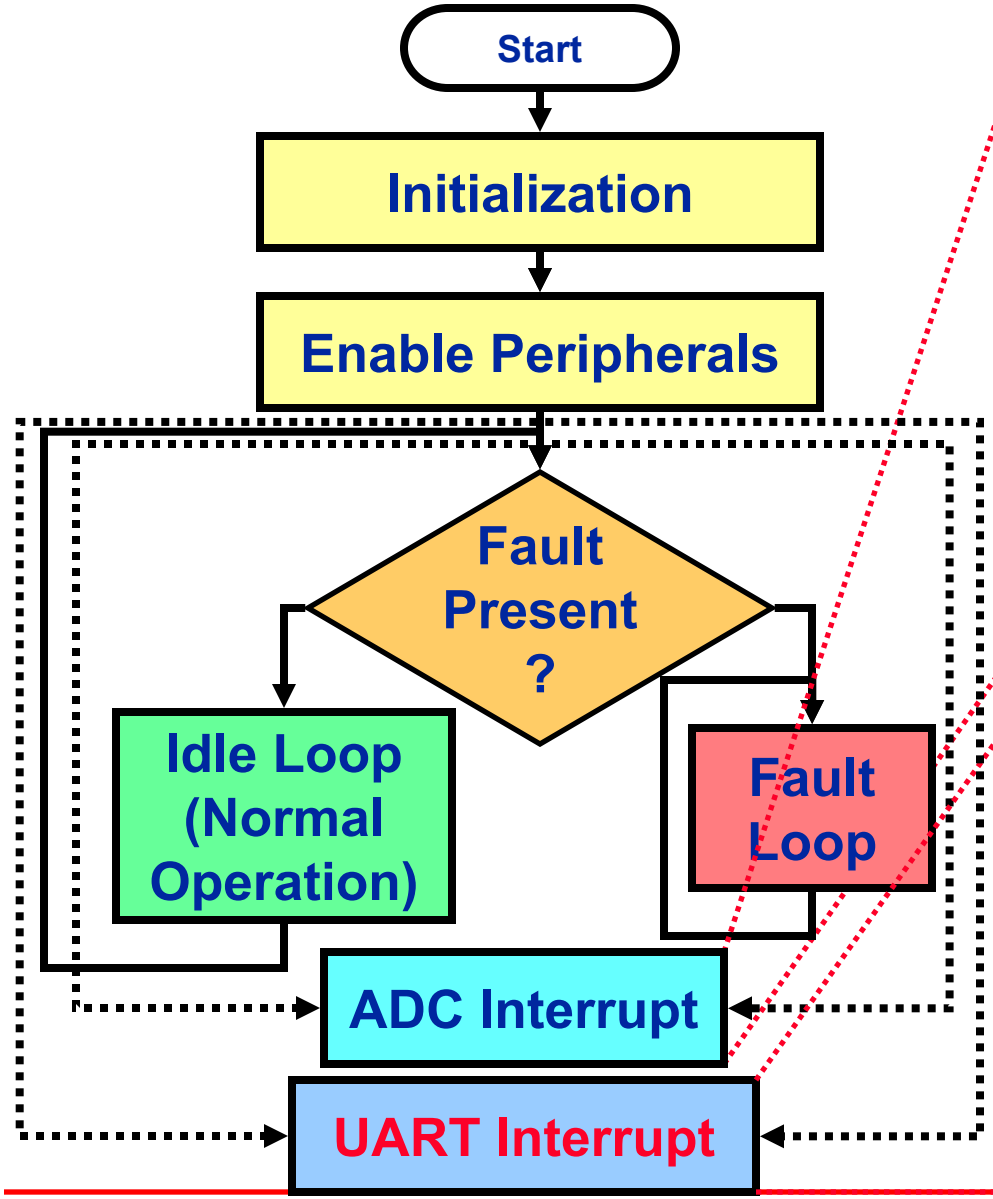
Structure of the ZVT Software



- **ADC Interrupt (High Priority)**
  - ZVT Current Loop
    - **ZVT Current Measurements**
    - **Check for Current Imbalance**
    - **Current PID Calculations**
    - **Update Phase Shift**

- **UART Interrupt (Medium Priority)**
  - ZVT Voltage Loop
    - **VOUT Measurement**
    - **ZVT Voltage PID Calculations**
    - **Update ZVT Current Reference**

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Additional Guidelines for Primary side dsPIC® DSC Software

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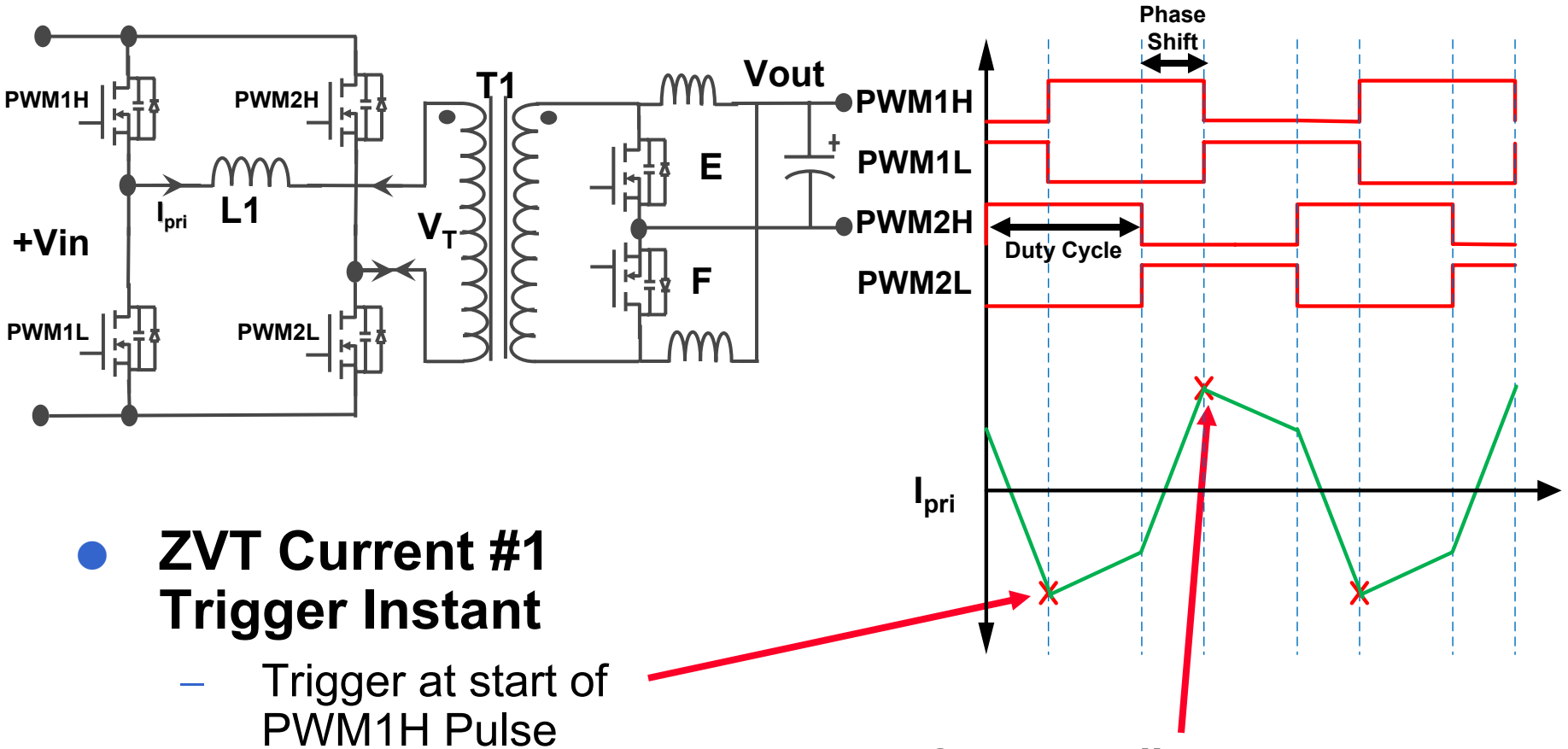
Full-Bridge Phase Shift ZVT Converter



- **ZVT Current #1 Trigger Instant**
  - Trigger at start of PWM1H Pulse

- **ZVT Current #2 Trigger Instant**
  - Trigger on PWM2H at (Duty Cycle + Phase Shift)

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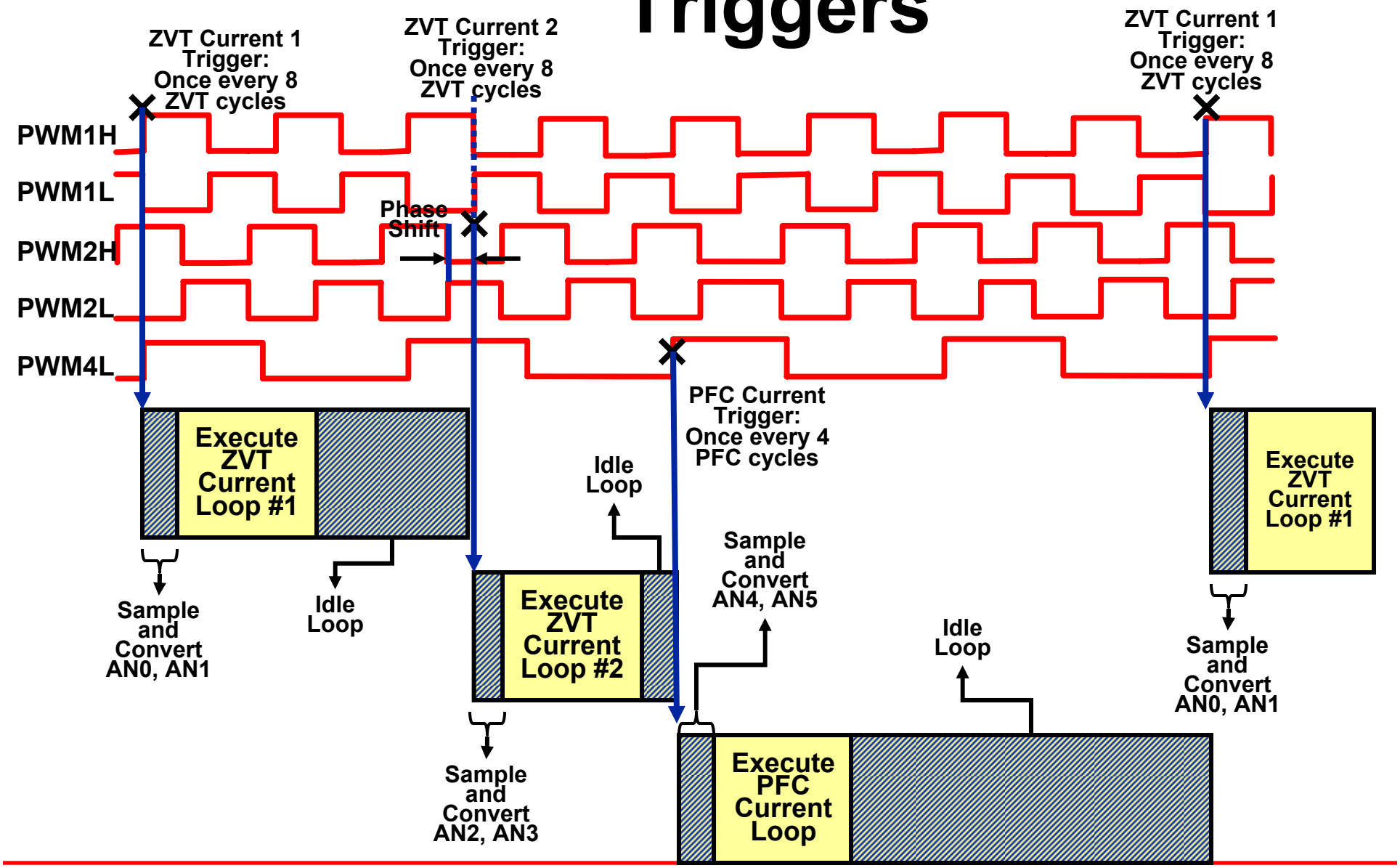
Sequence of Current Loop Triggers



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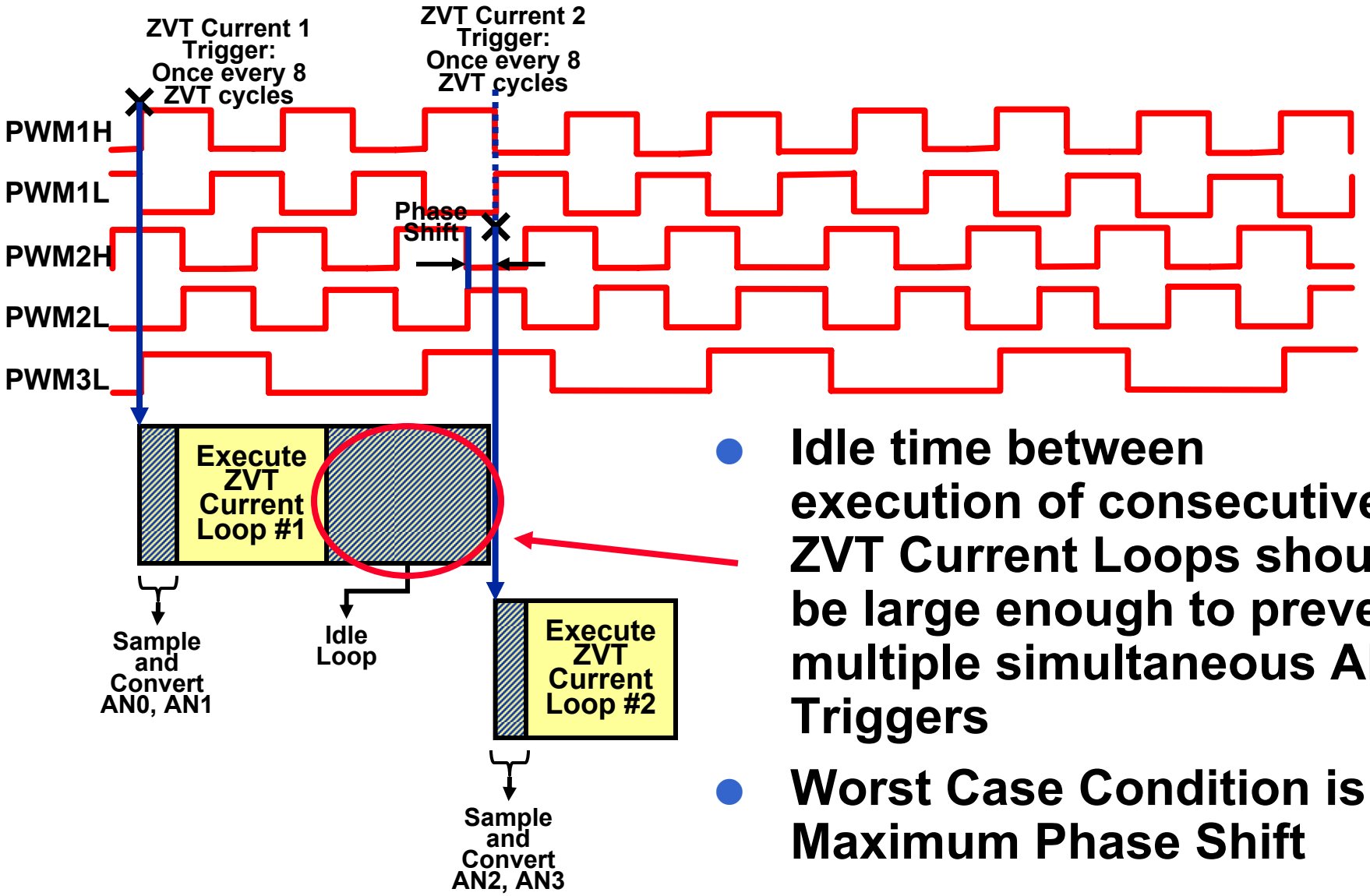
Time Management



- Idle time between execution of consecutive ZVT Current Loops should be large enough to prevent multiple simultaneous ADC Triggers
- Worst Case Condition is Maximum Phase Shift

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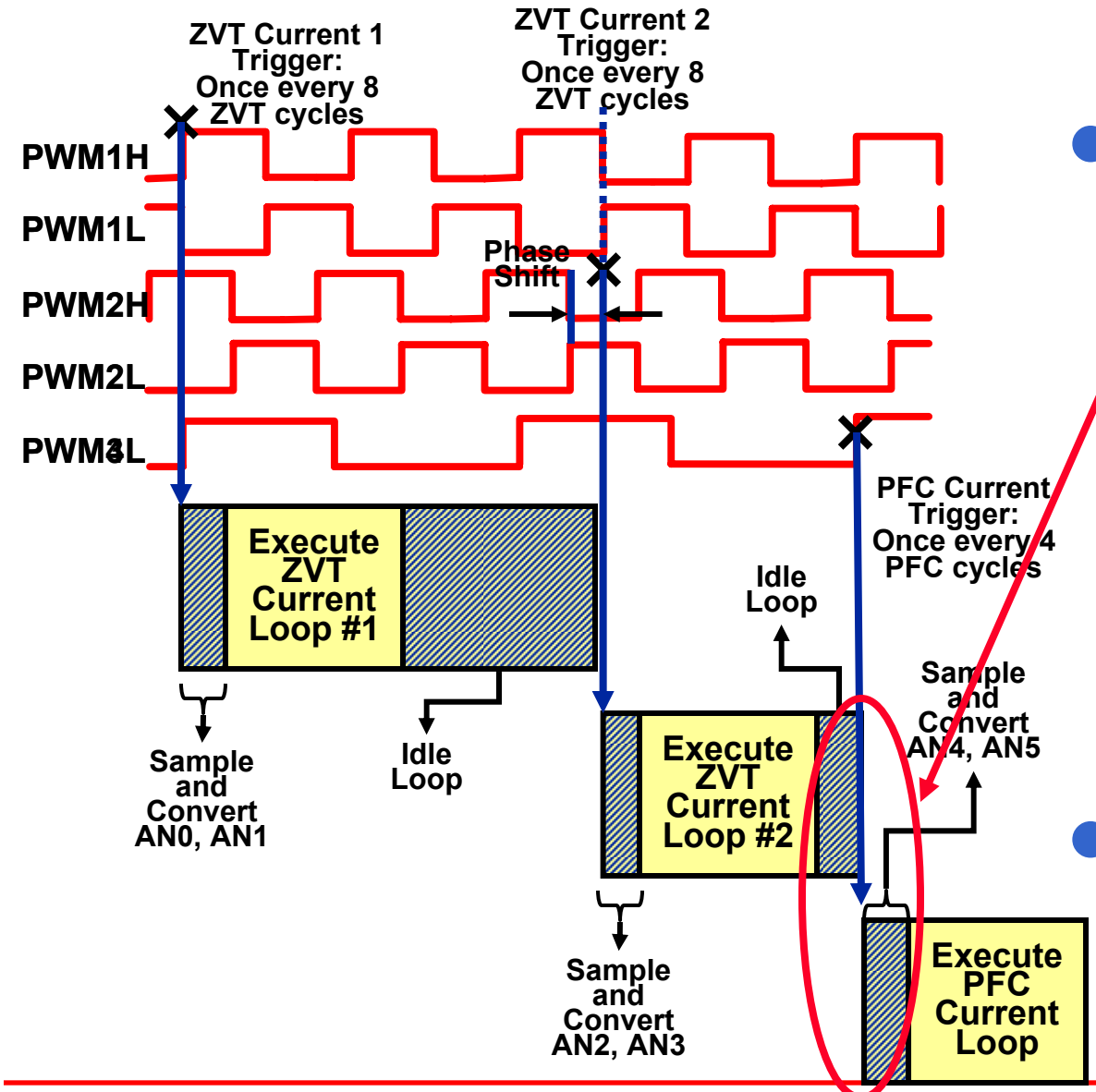
Time Management



- The Idle time after execution of the second ZVT Current Loop should be enough to prevent multiple simultaneous ADC Triggers
- Worst Case condition is zero Phase Shift

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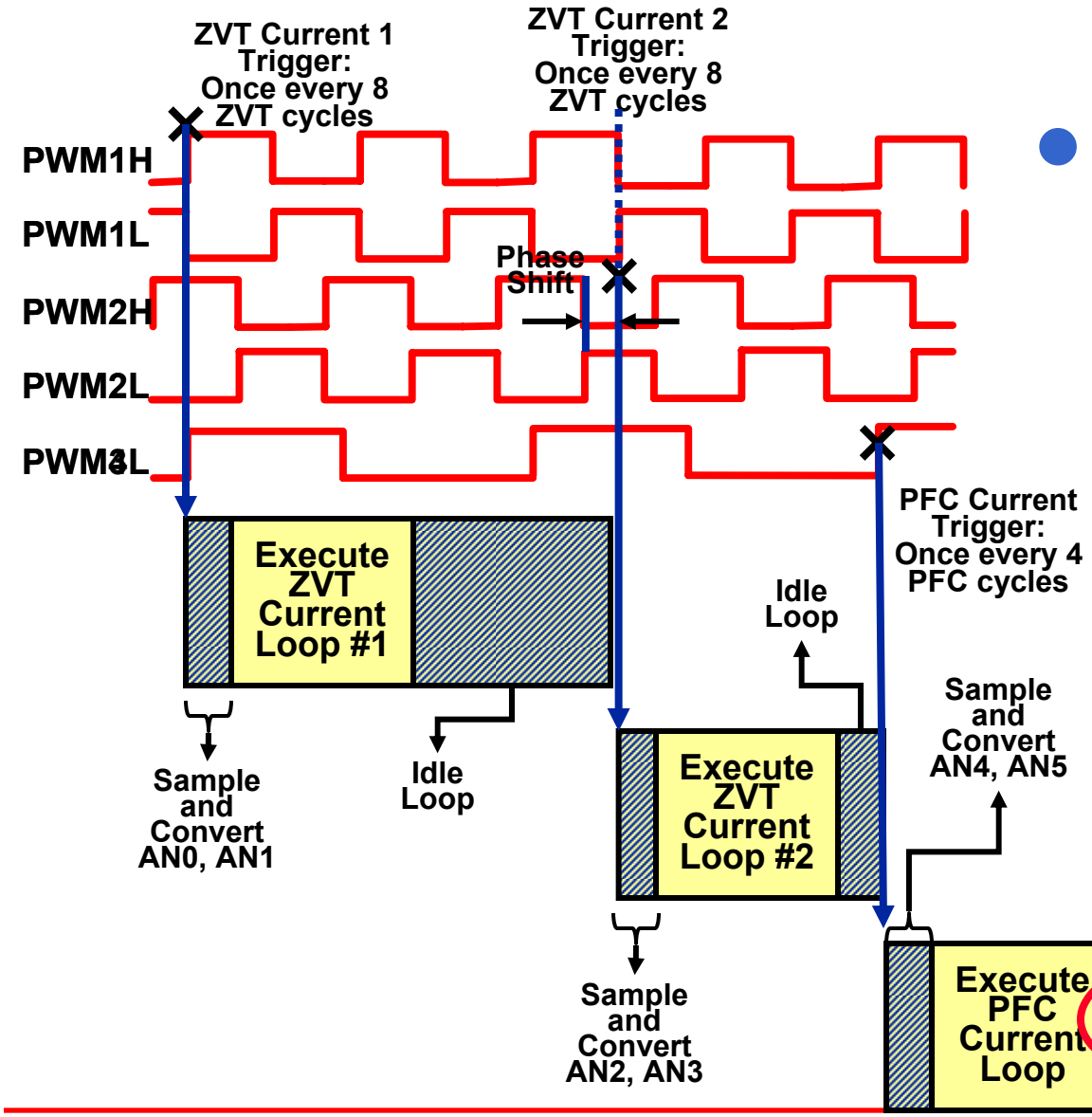
Time Management



- **The Idle time after PFC Current Loop Execution utilized for executing the Voltage Loops and auxiliary functions**

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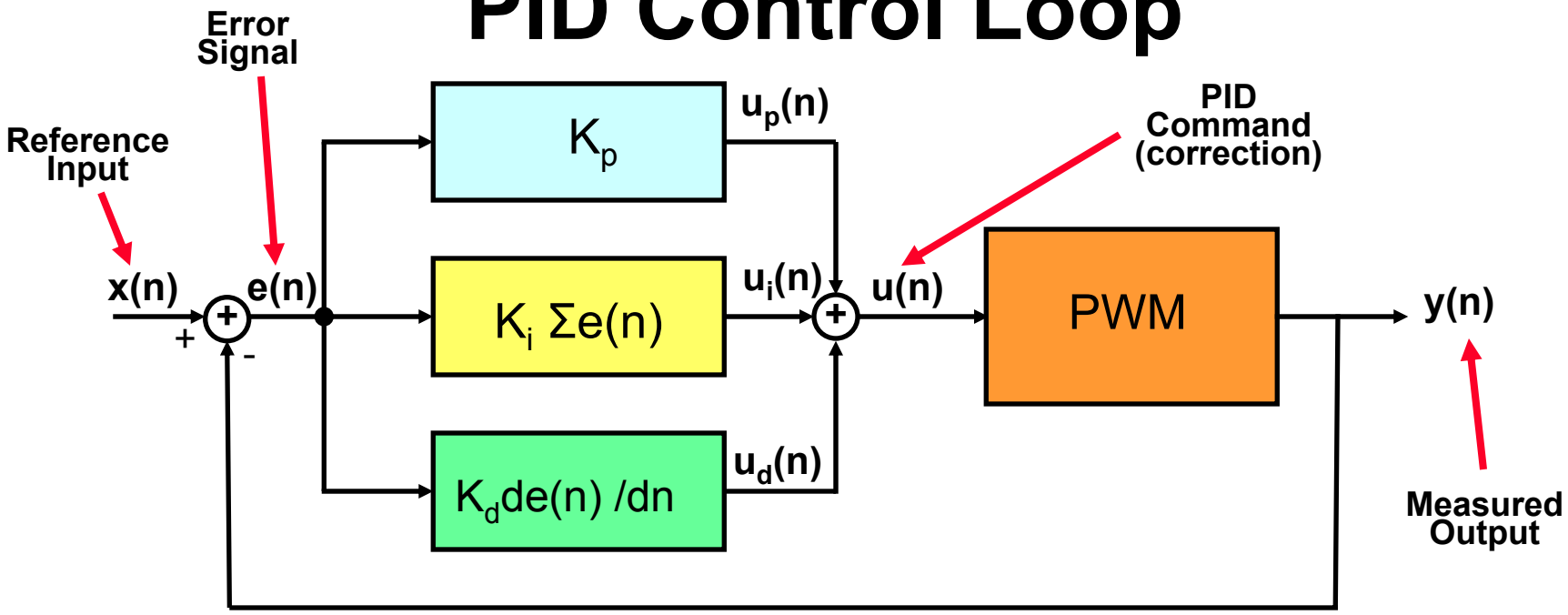
Control Loop Execution

PID Control Loop



$$u(n) = u_p(n) + u_i(n) + u_d(n)$$

where,

$$u_p(n) = K_p * e(n)$$

$$u_i(n) = K_i * [e(n) + e(n-1)]$$

$$u_d(n) = K_d * [e(n) - e(n-1)]$$

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Auxillary Tasks

- AC Input Voltage Measurement
- Check if Soft Start is required
- Temperature Measurement
- Communication Routines

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Demonstration #2

ZVT Operation

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Summary

- **Power Factor Correction**
  - Overview of PFC
  - Control Scheme for Digital PFC
  - Structure of Control Software
- **Zero Voltage Transition**
  - ZVS and ZCS and Full-Bridge Converter
  - ZVT Phase Shift Converter
  - Control Scheme for ZVT Converter
  - Structure of Control Software
- **Additional Guidelines for Primary Side dsPIC® DSC Control Software**
  - Time Management

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Agenda

- **Overview of AC/DC Reference Design**
- **AC/DC Reference Design Architecture**
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- **Multi-phase Buck Converters**
  - Multi-phase Buck Control Software
- **Enhanced Features**

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Multi-Phase Buck Converter

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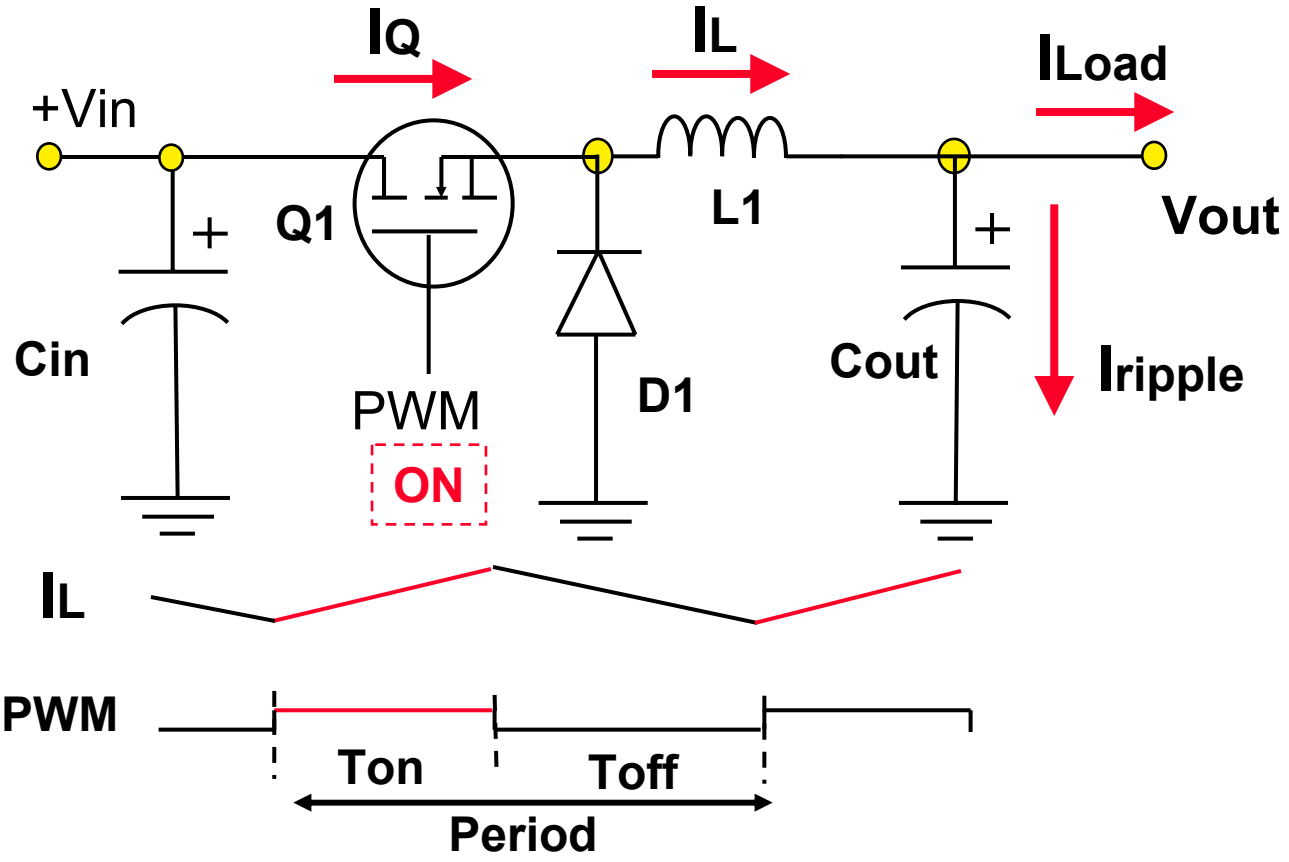
Basic Theory of a Buck Converter

Switch ON

Charging inductor

Step down converter



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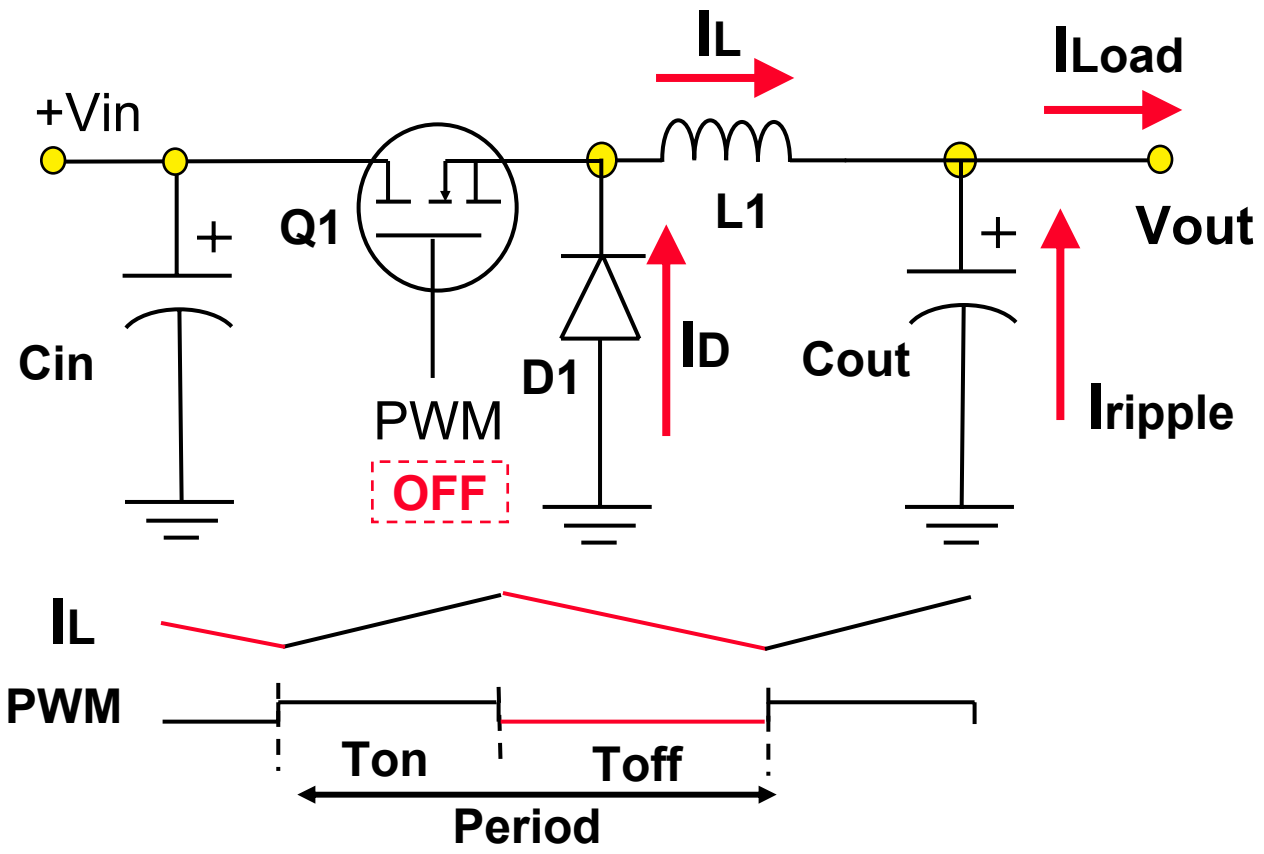
Basic Theory of a Buck Converter

Switch OFF

Discharging inductor

Step down converter



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PWM Pulse Width vs. Buck Output Voltage

$$Vout = Vin \bullet D$$

Where:

D = PWM dutycycle = Ton / (Ton +Toff)

Note: range of duty cycle = 0 to 1

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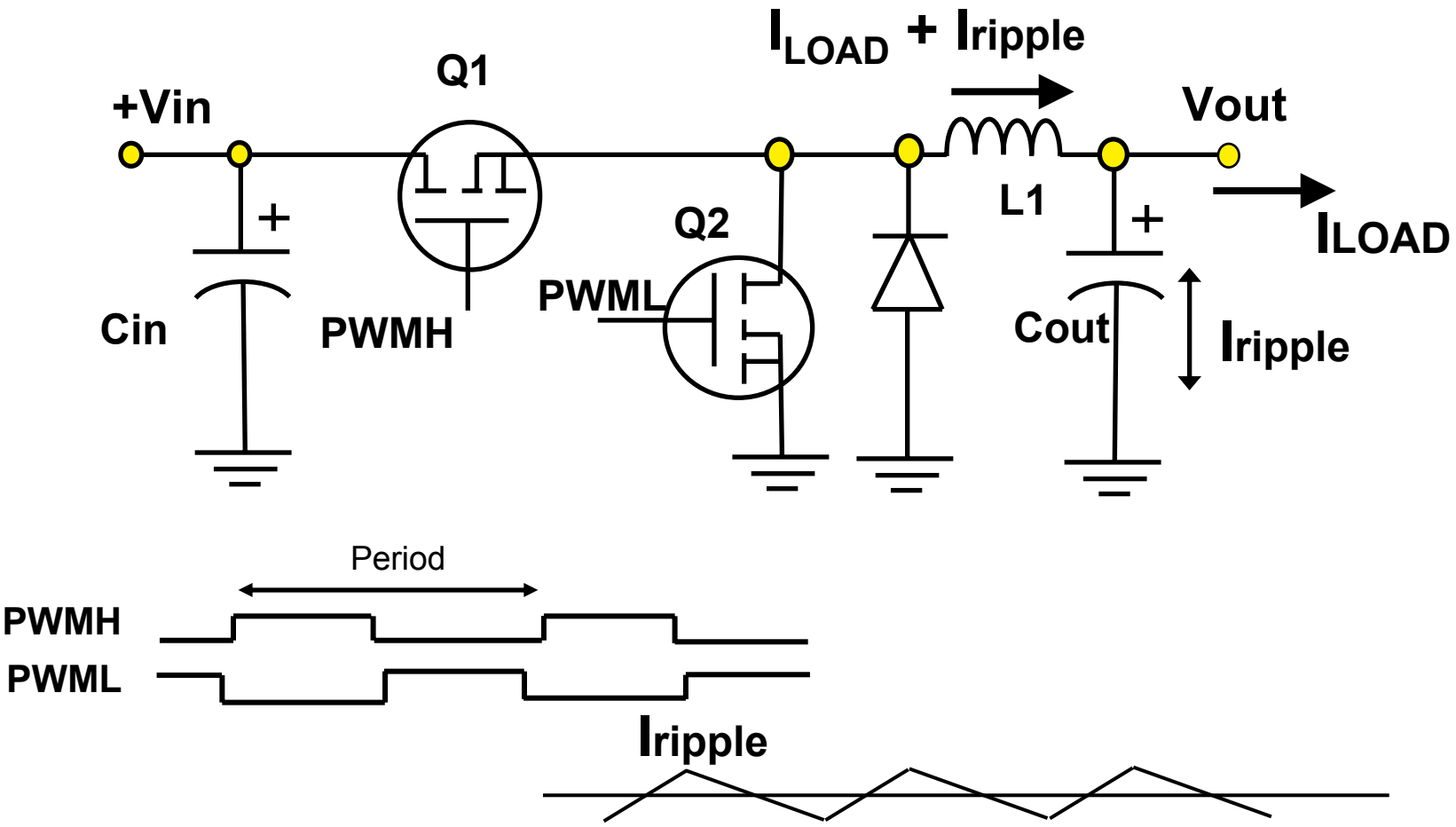
Synchronous Buck Converter



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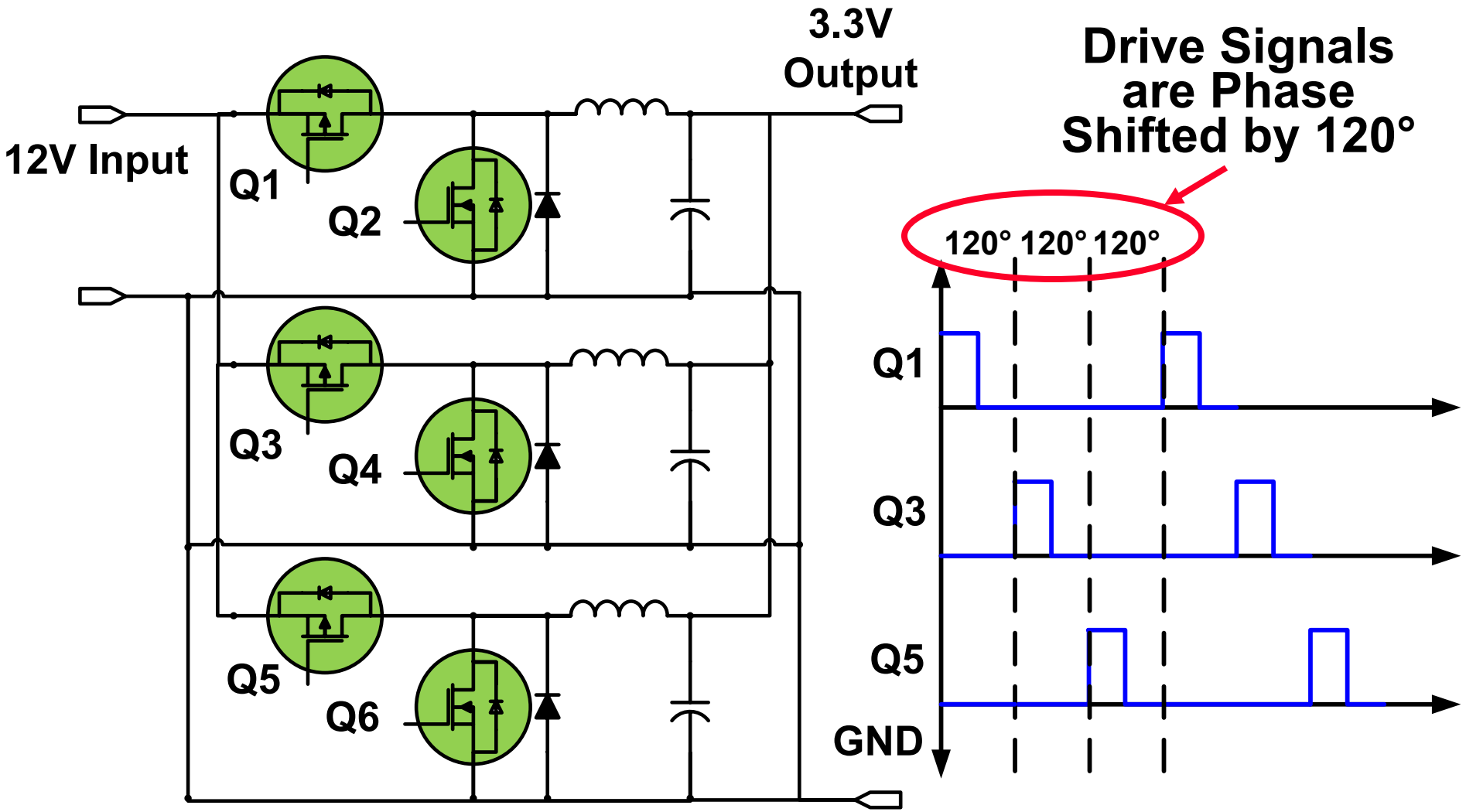
Multi-Phase Buck Converter



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Why the Multi-phase Buck Converter?

- Each Phase is rated for less Power
- Semiconductor Devices have lower current rating
- Smaller MOSFETs usually mean better switching speed
- Higher Output Ripple Frequency decreases size of output filter
- Ripple magnitude is reduced

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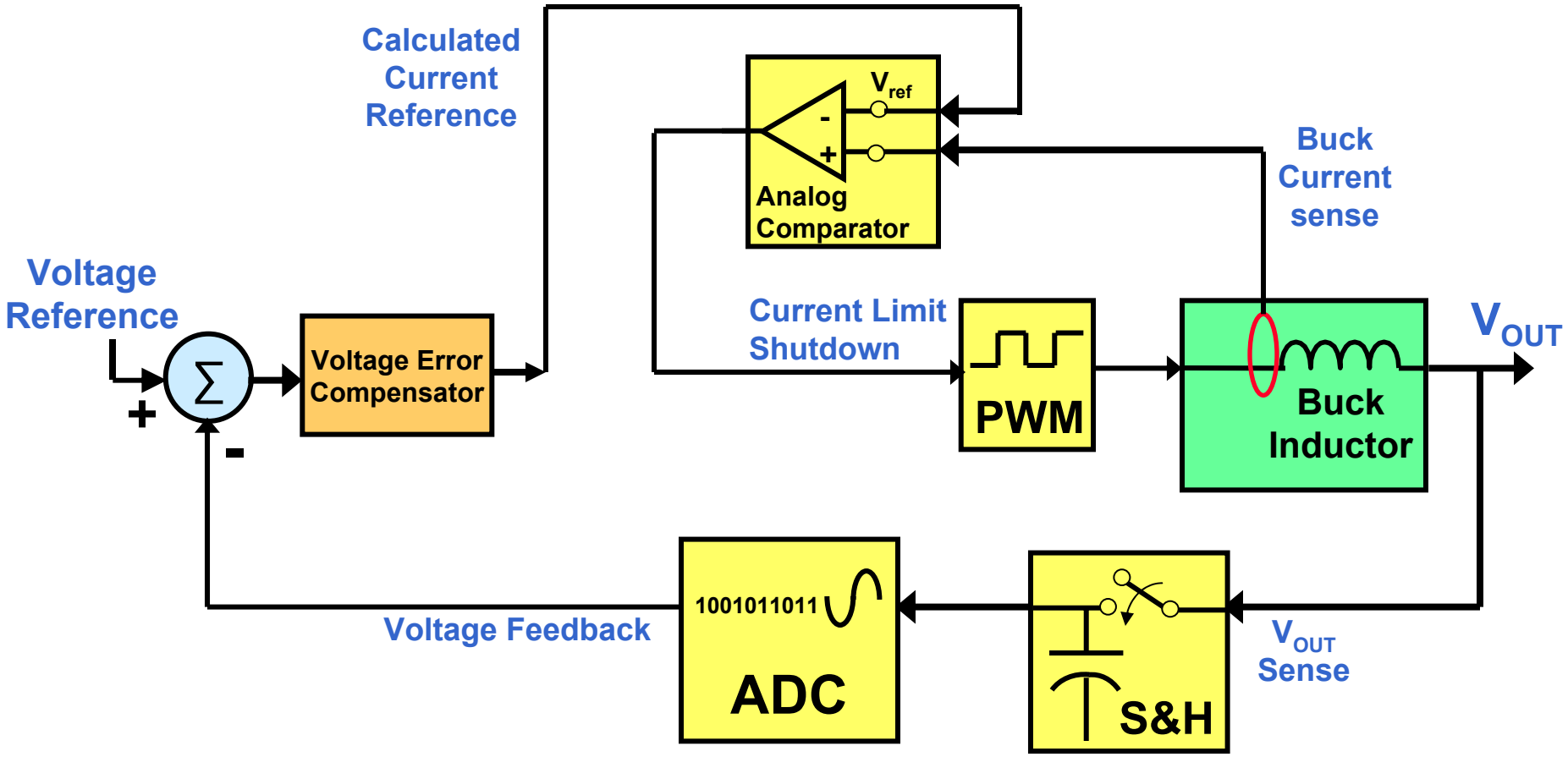
5V Buck Converter Control Scheme



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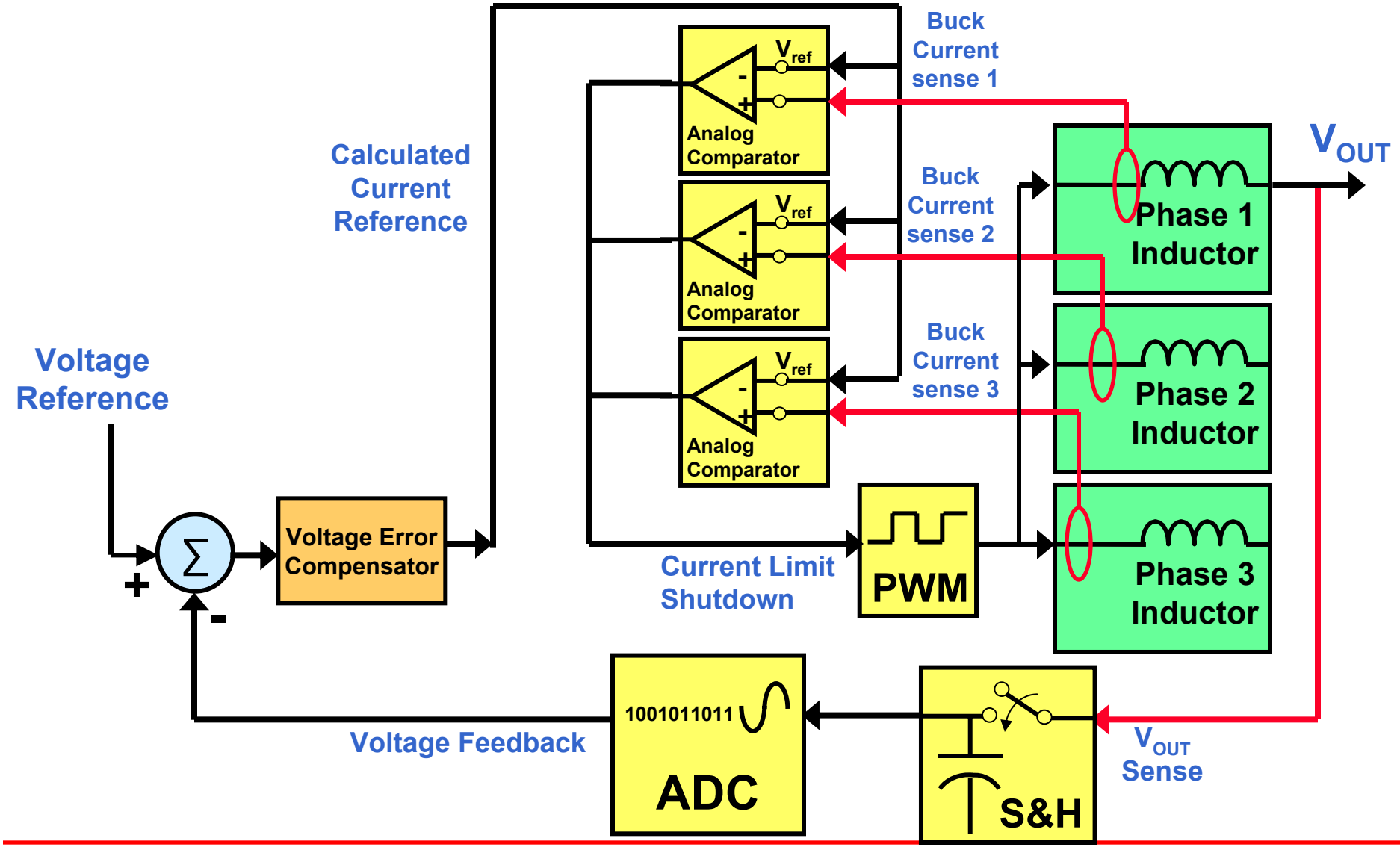
3.3V Buck Converter Control Scheme



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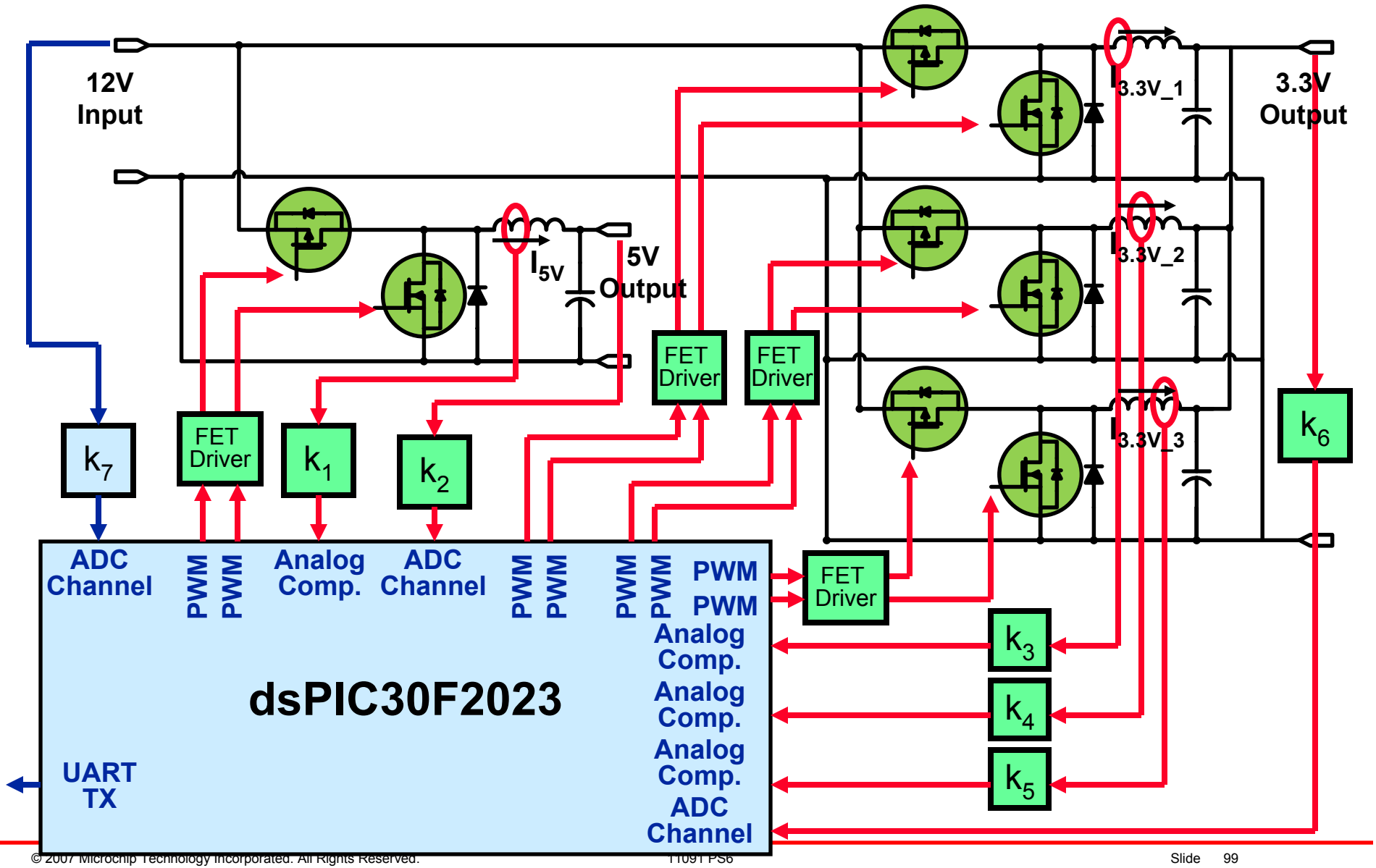
Resources Required for Digital Buck Converters



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Buck Converters Resource Allocation

Signal Name	Type of Signal	dsPIC® DSC Resource Used
I_{5V}	Analog Input	CMP1A
5V Output	Analog Input	AN1
$I_{3.3V\_1}$	Analog Input	CMP2A
$I_{3.3V\_2}$	Analog Input	CMP3A
$I_{3.3V\_3}$	Analog Input	CMP4A
3.3V Output	Analog Input	AN3
5V Buck Gate Drive	Drive Outputs	PWM4H, PWM4L

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Buck Converters Resource Allocation

Signal Name	Type of Signal	dsPIC® DSC Resource Used
3.3V Buck Gate Drive	Drive Outputs	PWM1H, PWM1L PWM2H, PWM2L PWM3H, PWM3L
5V Current Loop Trigger	dsPIC® DSC Internal Signal	PWM4 Trigger to Sample 5V Buck Voltage
3.3V Current Loop Trigger	dsPIC® DSC Internal Signal	PWM1 Trigger to Sample 3.3V Buck Voltage
12V Bus Sense	Analog Input	AN5
12V Digital Feedback	UART Transmission	U1TX
Temperature Sense	Analog Input	AN8

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Agenda

- **Overview of AC/DC Reference Design**
- **AC/DC Reference Design Architecture**
- **Power Factor Correction**
  - PFC Control Software
- **Zero Voltage Transition**
  - ZVT Control Software
- **Multi-phase Buck Converters**
  - Multi-phase Buck Control Software
- **Enhanced Features**

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Multi-Phase Buck Converter Control Software

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Multi-Phase Buck Converter Software Overview

- ADC Conversions are initiated by the PWM Trigger Feature
- Peak Current Control is implemented using the Analog Comparators
  - Additional Check Desired for Current Imbalance between the three phases
- The Voltage and Current Loops are executed at the same speed
- The UART Transmission for 12V digital feedback is executed from a Timer Interrupt

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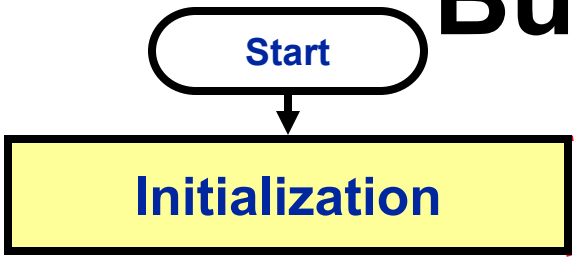
Structure of the Multi-Phase Buck Software



- Initialize PWM
- Initialize ADC
- Initialize Analog Comparators
- Setup Timers
- Configure UART
- Configure Interrupts
- Initialize Control Loop Variables

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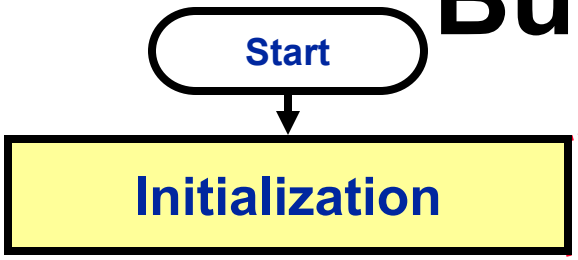
Structure of the Multi-Phase Buck Software



- **Initialize PWM**
  - Configure PWM Mode, Output Polarity, Period, Duty Cycle and Phase Shift
  - Setup PWM Current Limit Sources
  - Setup PWM Triggers

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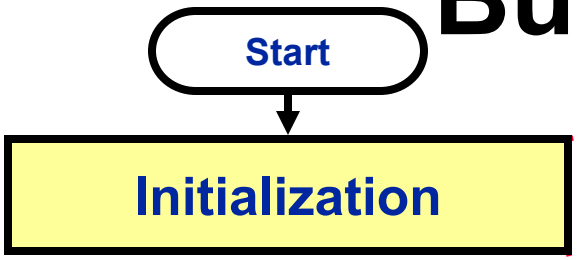
Structure of the Multi-Phase Buck Software



- **Initialize ADC**
  - Setup ADC Speed
  - Configure desired ADC channels as analog inputs
  - Choose ADC Trigger Sources
  - Configure ADC Data Format
  - Choose Simultaneous or Sequential Sampling

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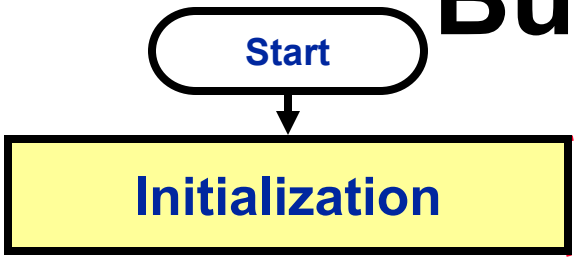
Structure of the Multi-Phase Buck Software



- **Initialize Analog Comparators**
  - Configure Correct Analog Comparator Inputs
  - Choose Voltage Reference Source
  - Setup Initial DAC Reference
  - Choose Comparator Output Polarity

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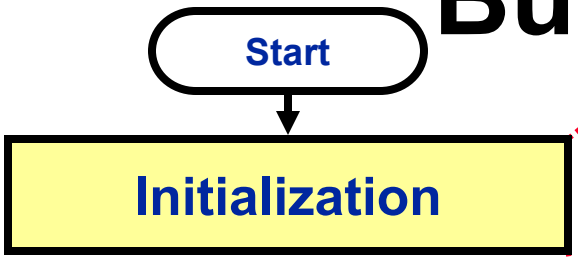
Structure of the Multi-Phase Buck Software



Configure UART

- Use UART to transmit 12V Bus Data to Primary Side dsPIC® DSC

Setup Interrupts

- PWM Interrupt for Fault Handling
- Timer Interrupt to trigger Voltage Control Loop
- ADC Interrupt to trigger Current Control Loop

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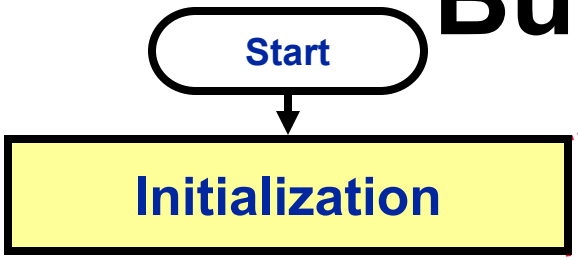
Structure of the Multi-Phase Buck Software



- **Initialize Control Loop Variables**
  - Initialize PID Gain Terms in X-memory
  - Initialize Measured signals in Y-memory
  - Initialize pointers to Control Loop Inputs and Outputs

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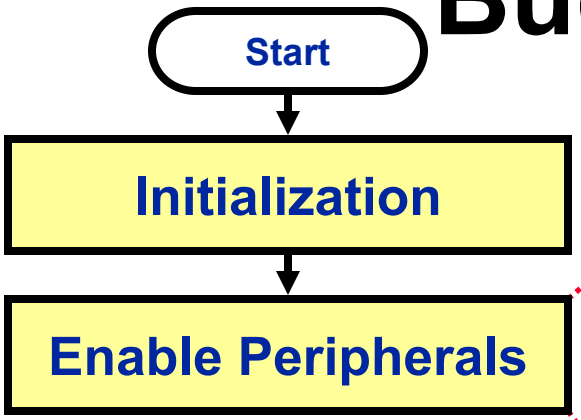
Structure of the Multi-Phase Buck Software



- **Enable Peripherals**
  - Enable Analog Comparators
  - Enable ADC
  - Enable PWM
  - Enable UART

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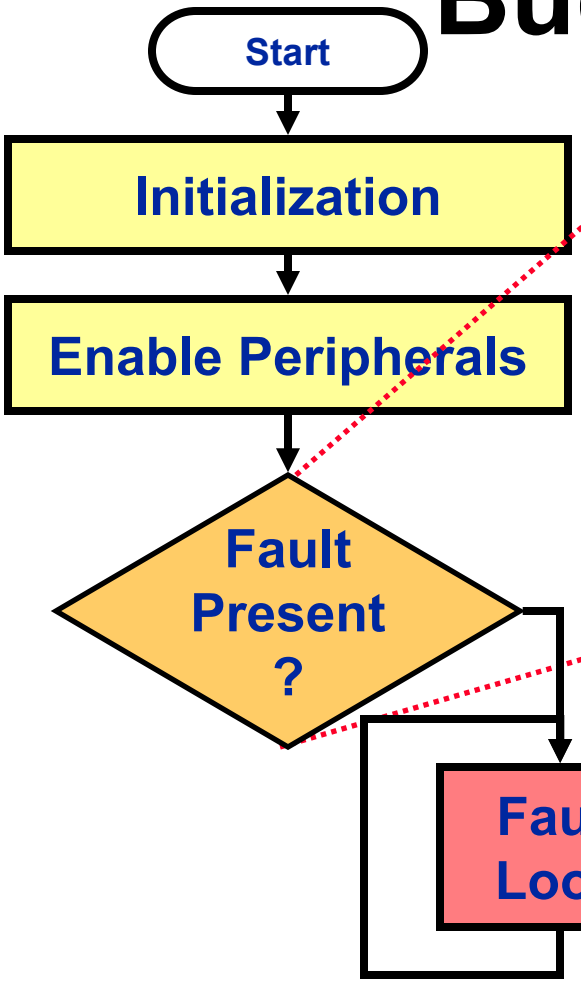
Structure of the Multi-Phase Buck Software



- **Check for Faults**
  - The PWM Module is setup to detect Faults and Shutdown all Outputs
  - The PWM Fault Interrupt sets the Fault Flag
  - The Main Routine Checks the Fault Flag

- **Fault Loop**
  - The Fault Indicator LED is enabled
  - Any other Fault Handling Routines can be placed in this loop

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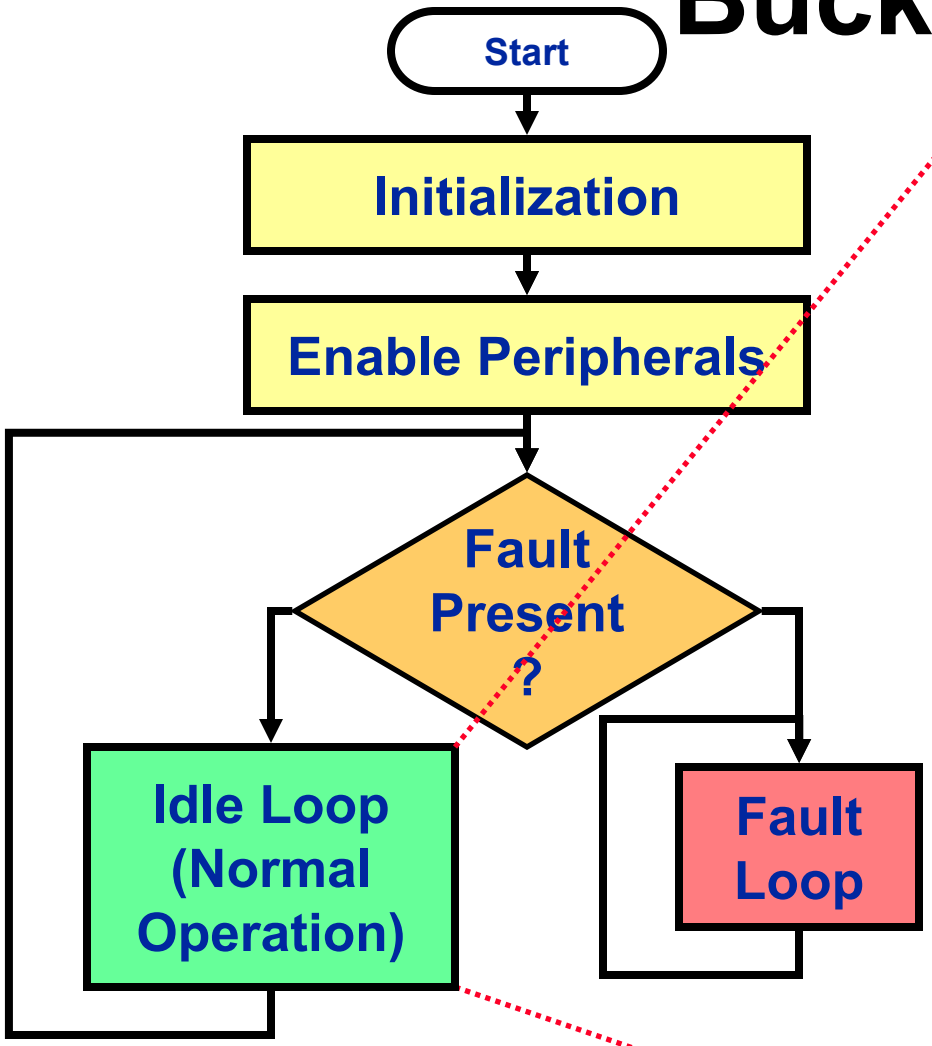
Structure of the Multi-Phase Buck Software



- **Idle Loop (Low Priority)**
  - Transmit 12V Bus Data
  - Power Management Routines
  - Check Temperature
  - Other Auxiliary Features

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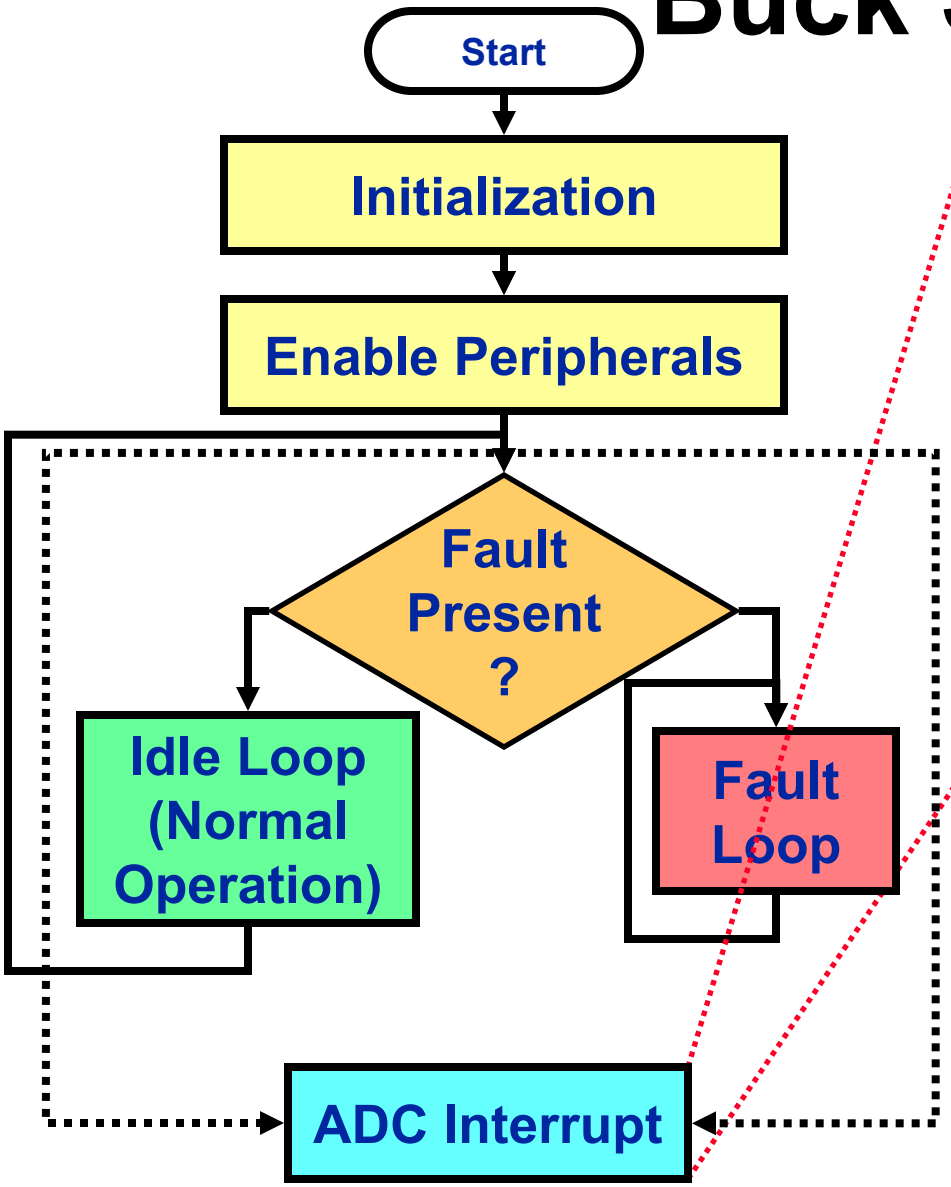
Structure of the Multi-Phase Buck Software



- **ADC Interrupt (High Priority)**
  - Buck Current Loop
    - **V_{OUT} Measurement**
    - **Calculate Current Reference**
    - **Update Analog Comparator DAC References**

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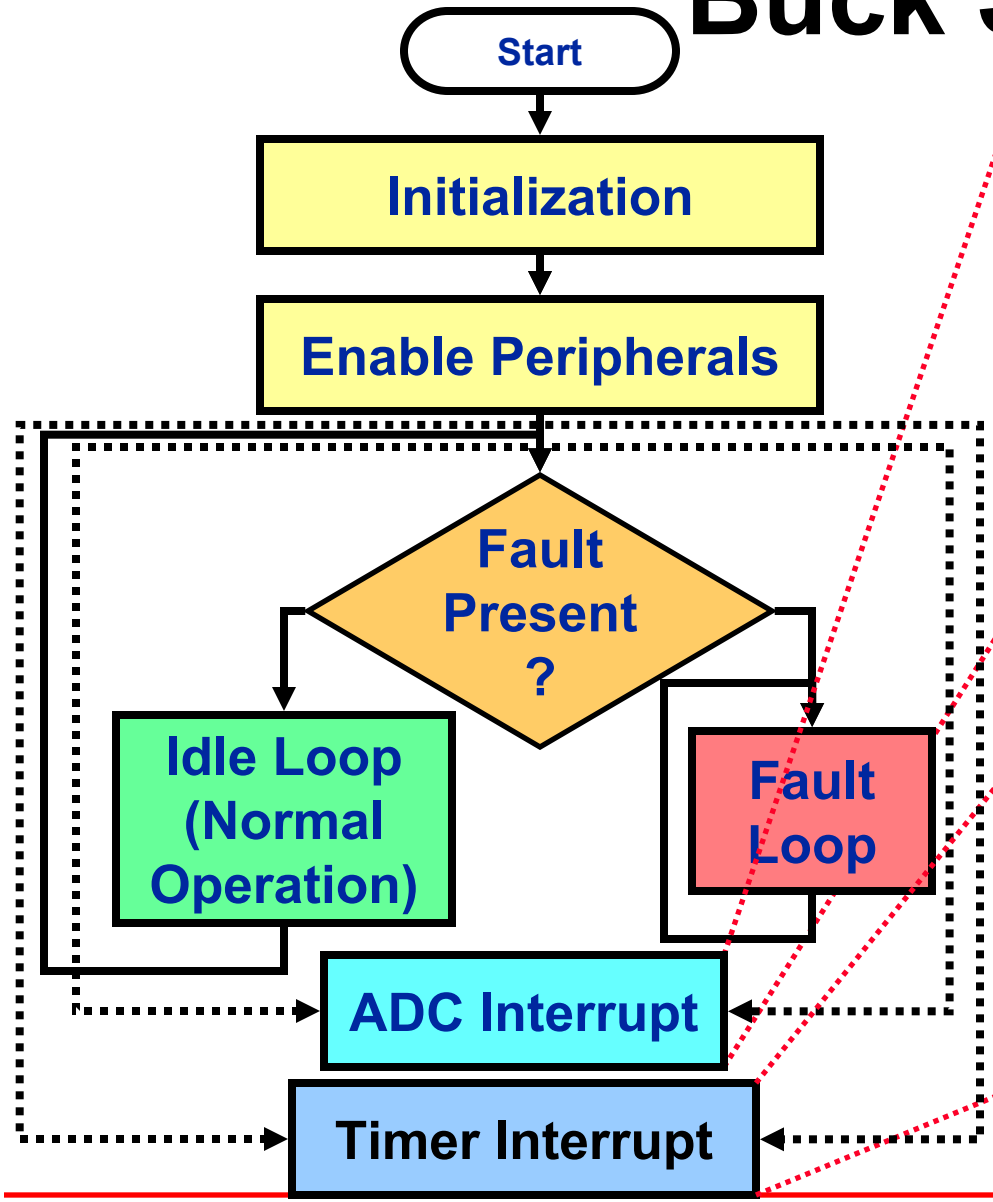
Structure of the Multi-Phase Buck Software



- **ADC Interrupt (High Priority)**
  - Buck Current Loop
    - **V_{OUT} Measurement**
    - **Calculate Current Reference**
    - **Update Analog Comparator DAC References**

- **Timer Interrupt (Medium Priority)**
  - Buck Voltage Loop
    - **Transmit 12V Digital Feedback Signal**

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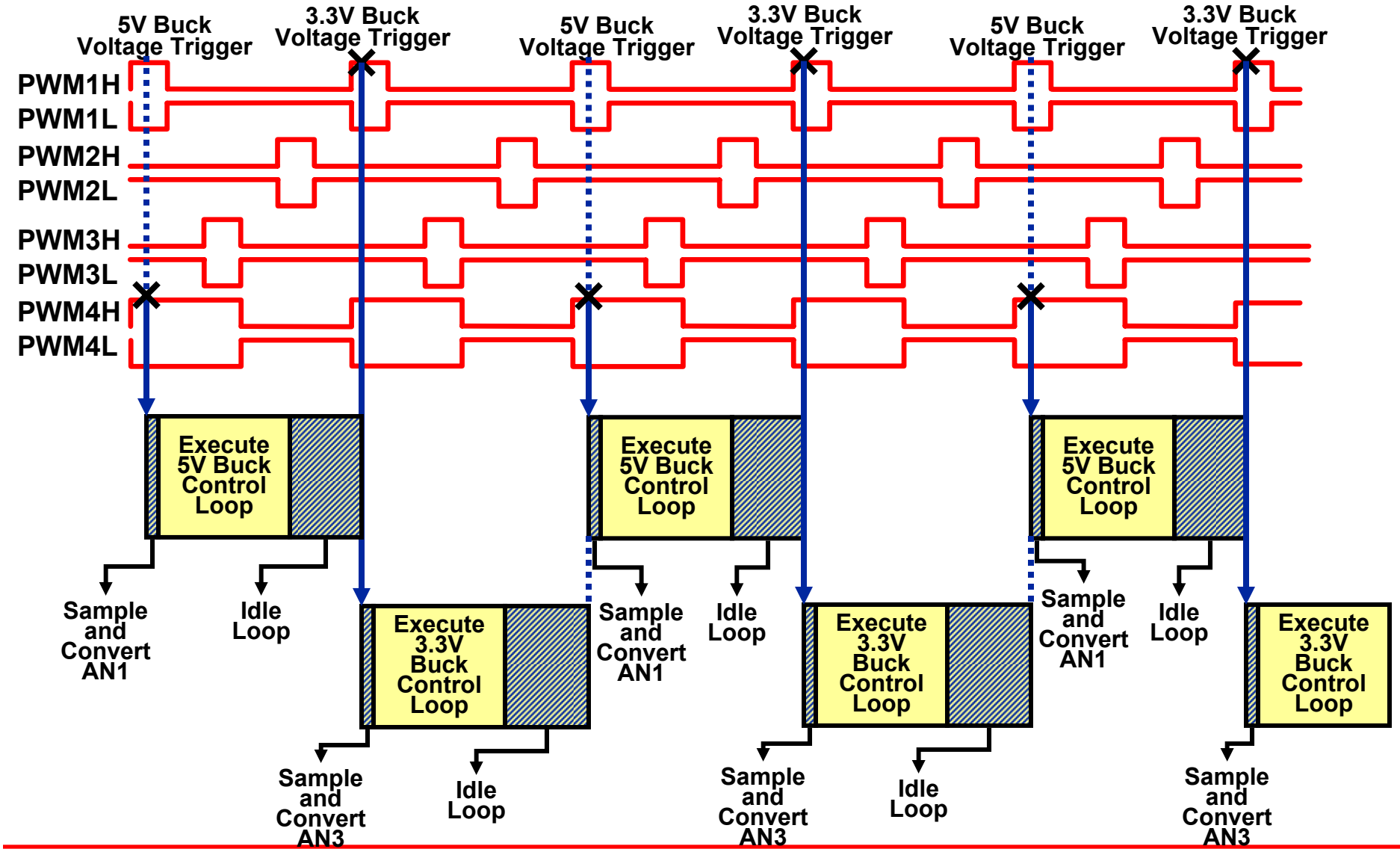
Sequence of Current Loop Triggers



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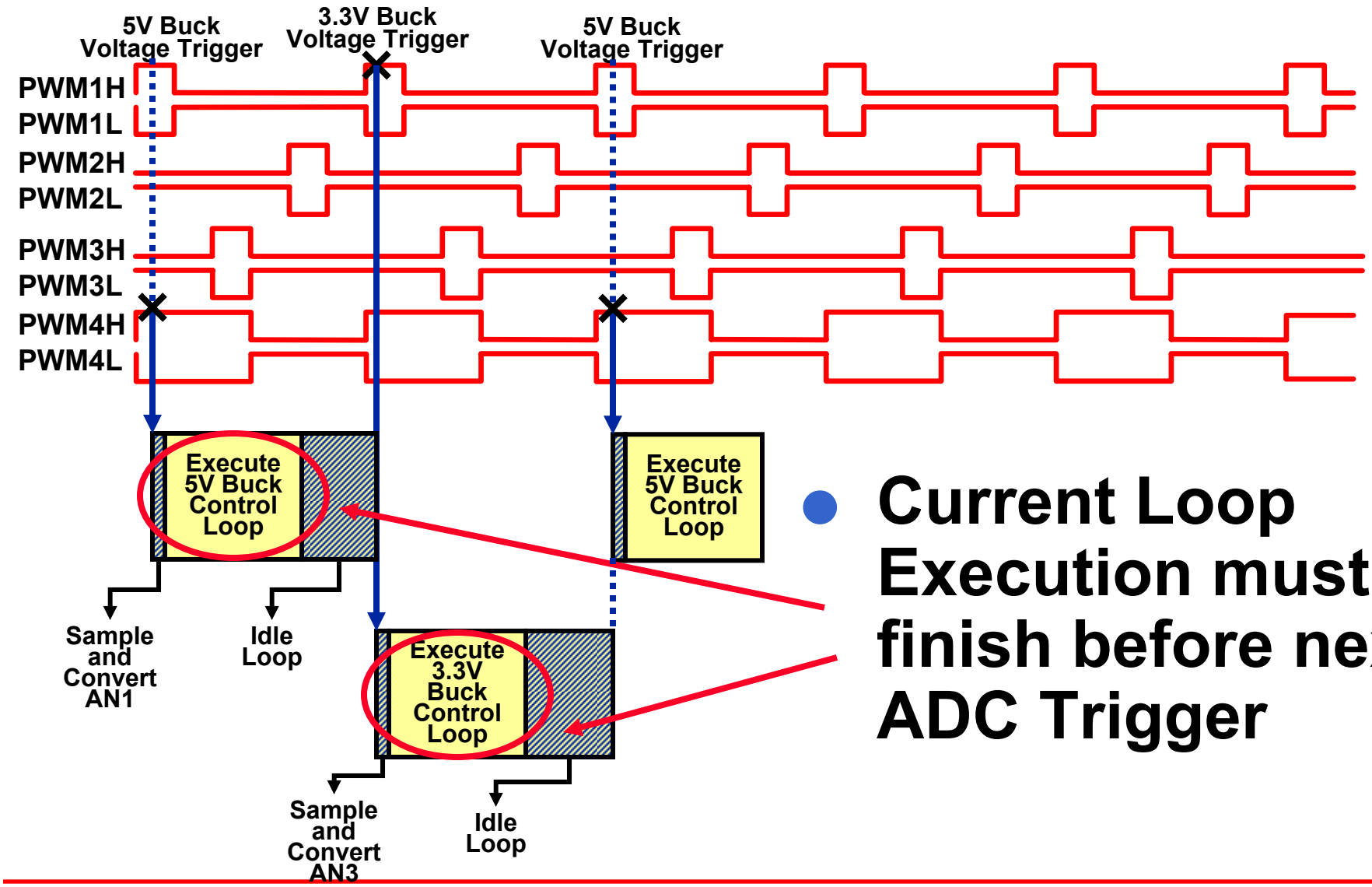
Sequence of Current Loop Triggers



- Current Loop Execution must finish before next ADC Trigger

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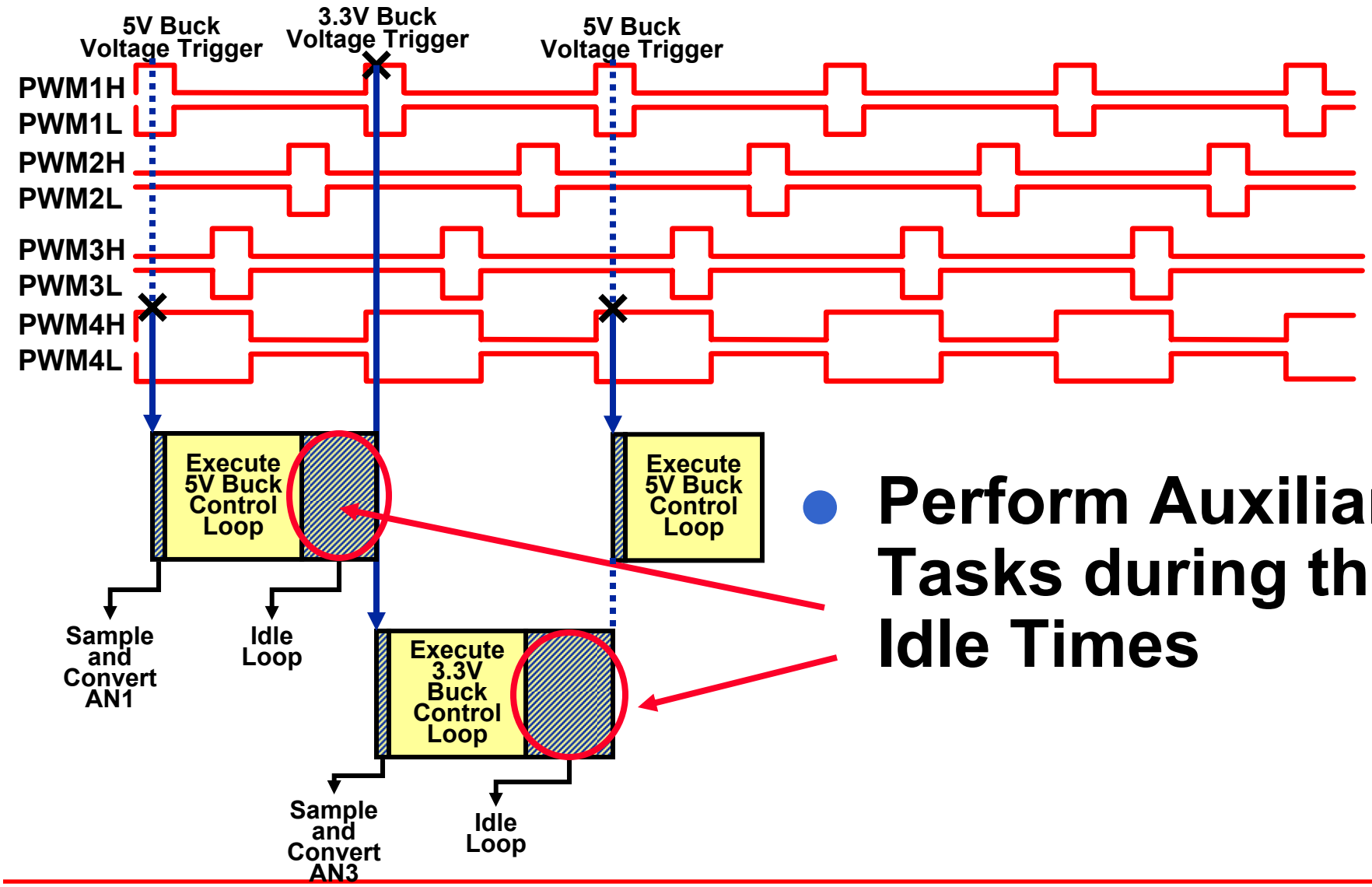
Sequence of Current Loop Triggers



- Perform Auxiliary Tasks during the Idle Times

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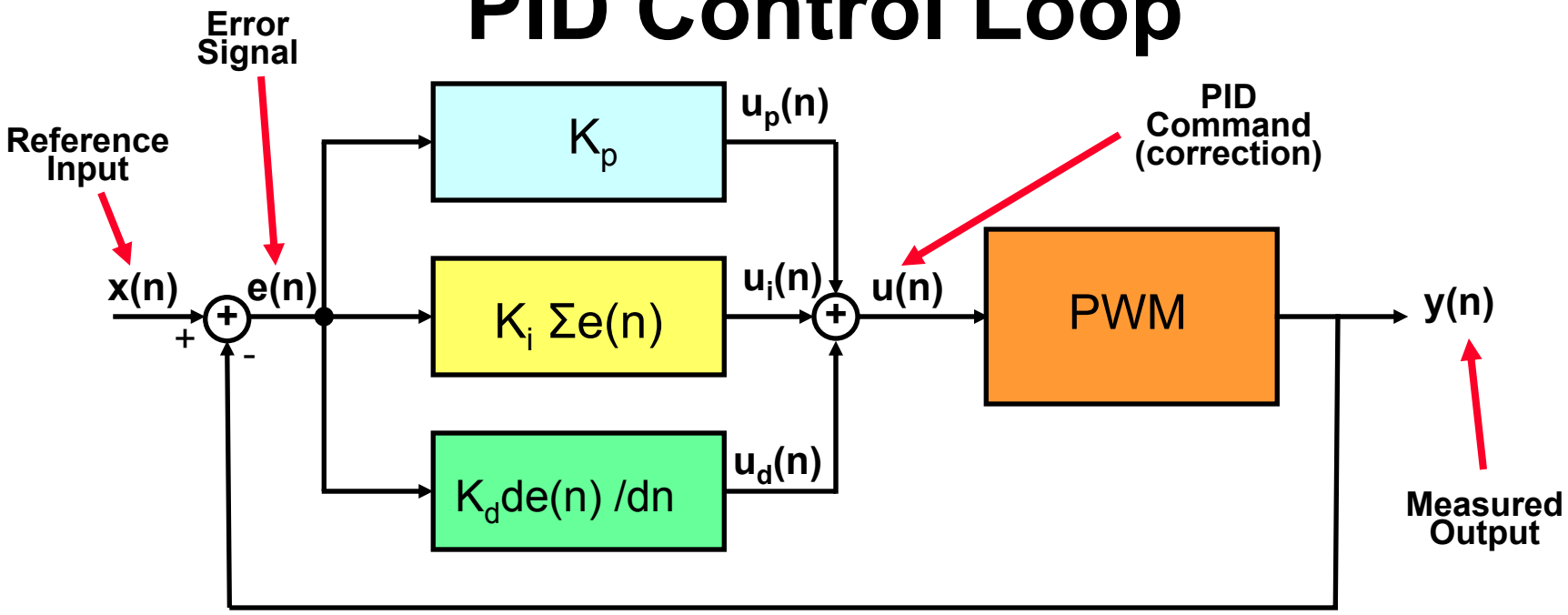
Control Loop Execution

PID Control Loop



$$u(n) = u_p(n) + u_i(n) + u_d(n)$$

where,

$$u_p(n) = K_p * e(n)$$

$$u_i(n) = K_i * [e(n) + e(n-1)]$$

$$u_d(n) = K_d * [e(n) - e(n-1)]$$

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Auxillary Tasks

- 12V Bus Voltage Measurement
- Communication Routines
- Load Sharing Routines
- Temperature Measurement
- Power Management Routines

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Demonstration #3

High Power Operation

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Enhanced Features

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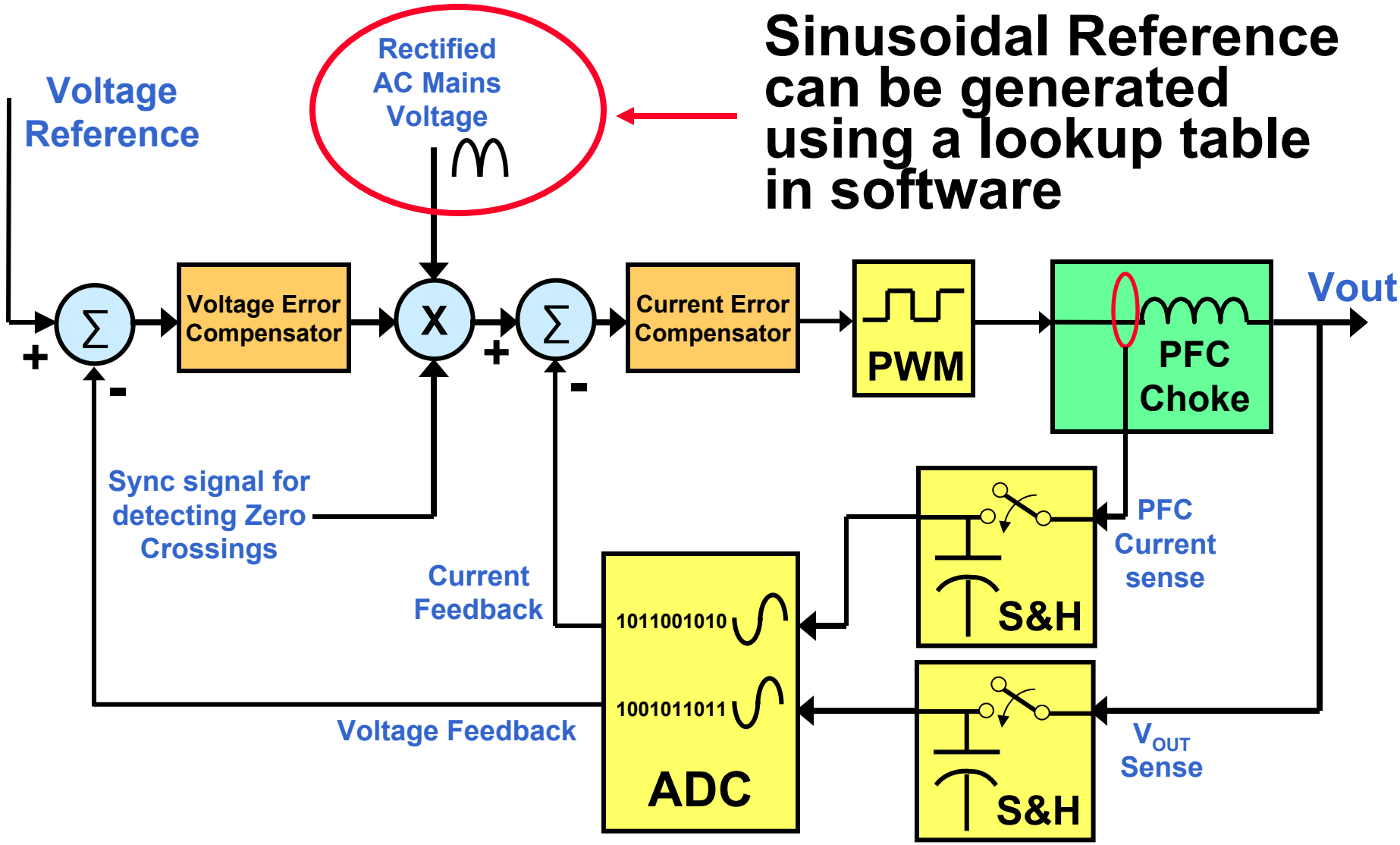
PFC Sinusoidal Reference



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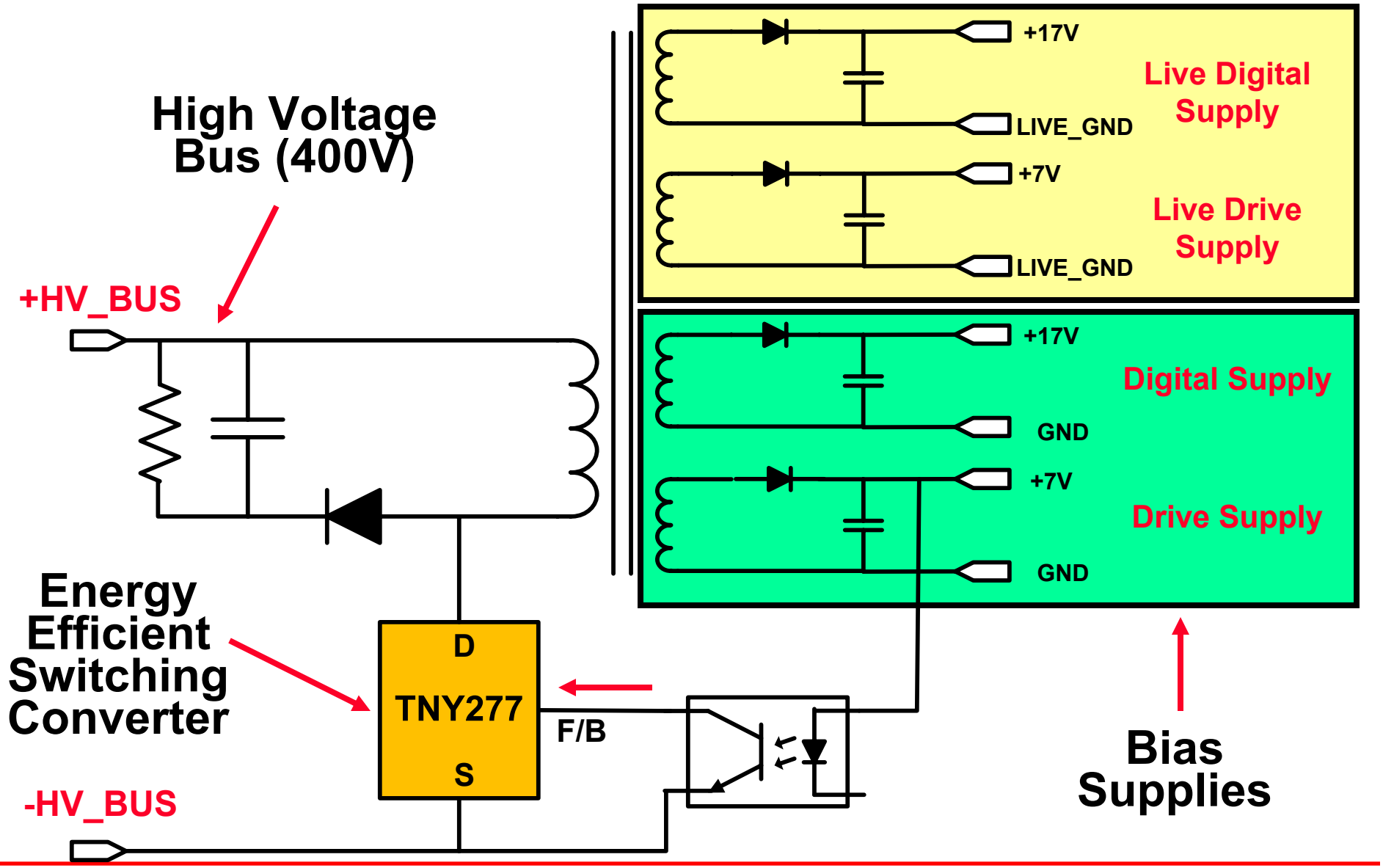
HV Bias Supply



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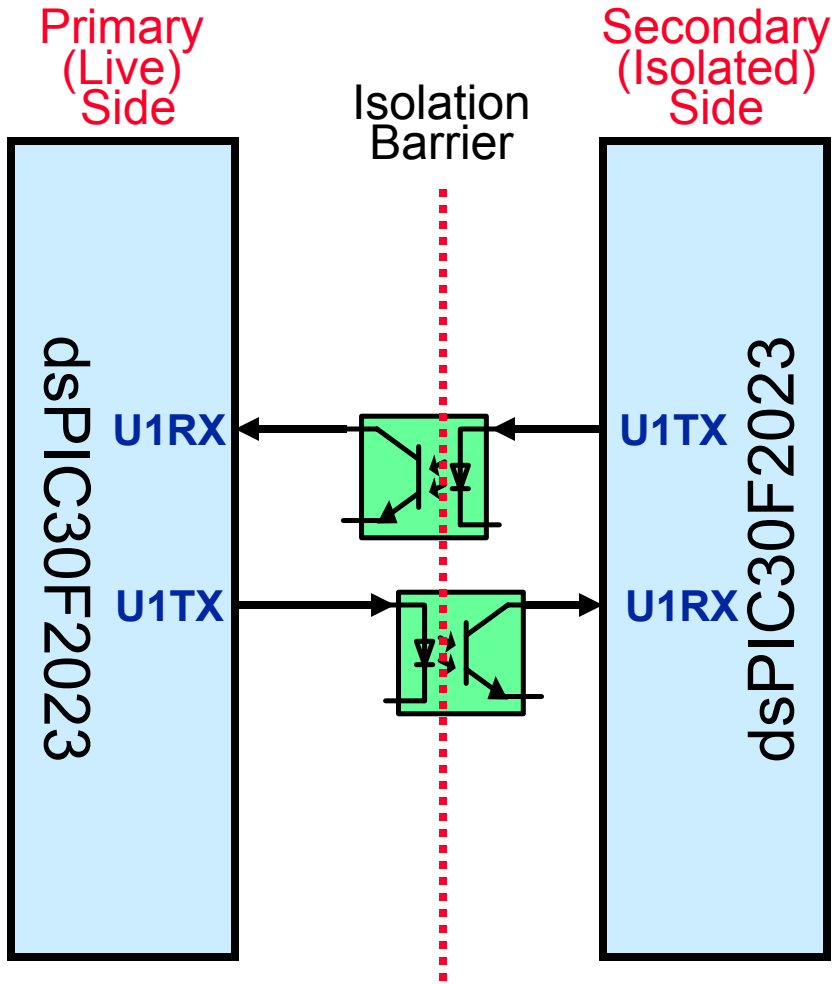
DSC to DSC Communication

- Perform status checks
- Report Fault Conditions to protect Hardware
- Implement Data Logging and Remote Monitoring



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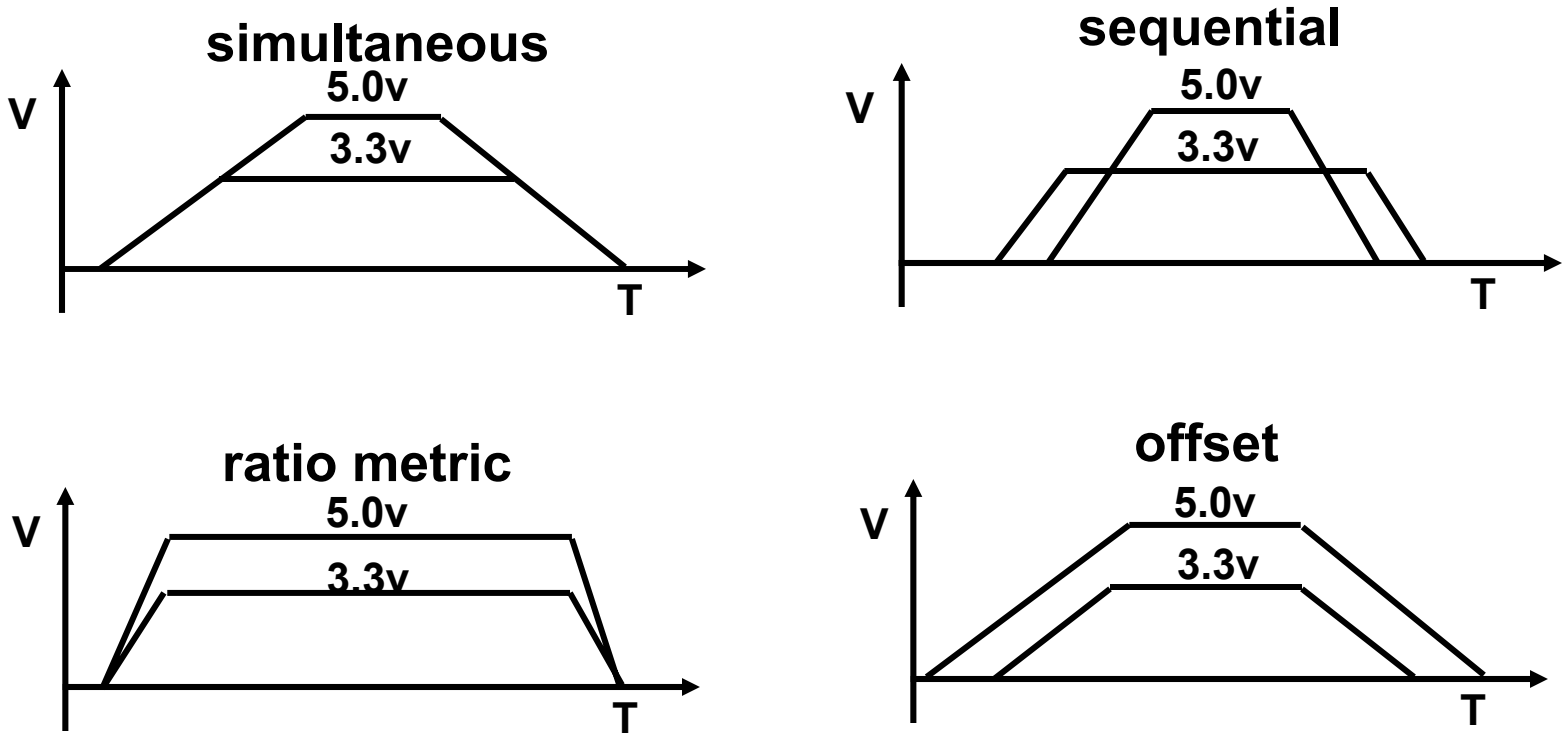
Power Supply Sequencing



- Choose method that meets system requirements

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Output Protection Schemes

- **A number of protection schemes can be implemented**
  - Constant Current Limiting
  - Constant Power Limiting
  - Output Over-voltage Shutdown
  - Input Under-voltage Shutdown
- **All shutdown schemes can be configured for immediate or delayed shutdown**

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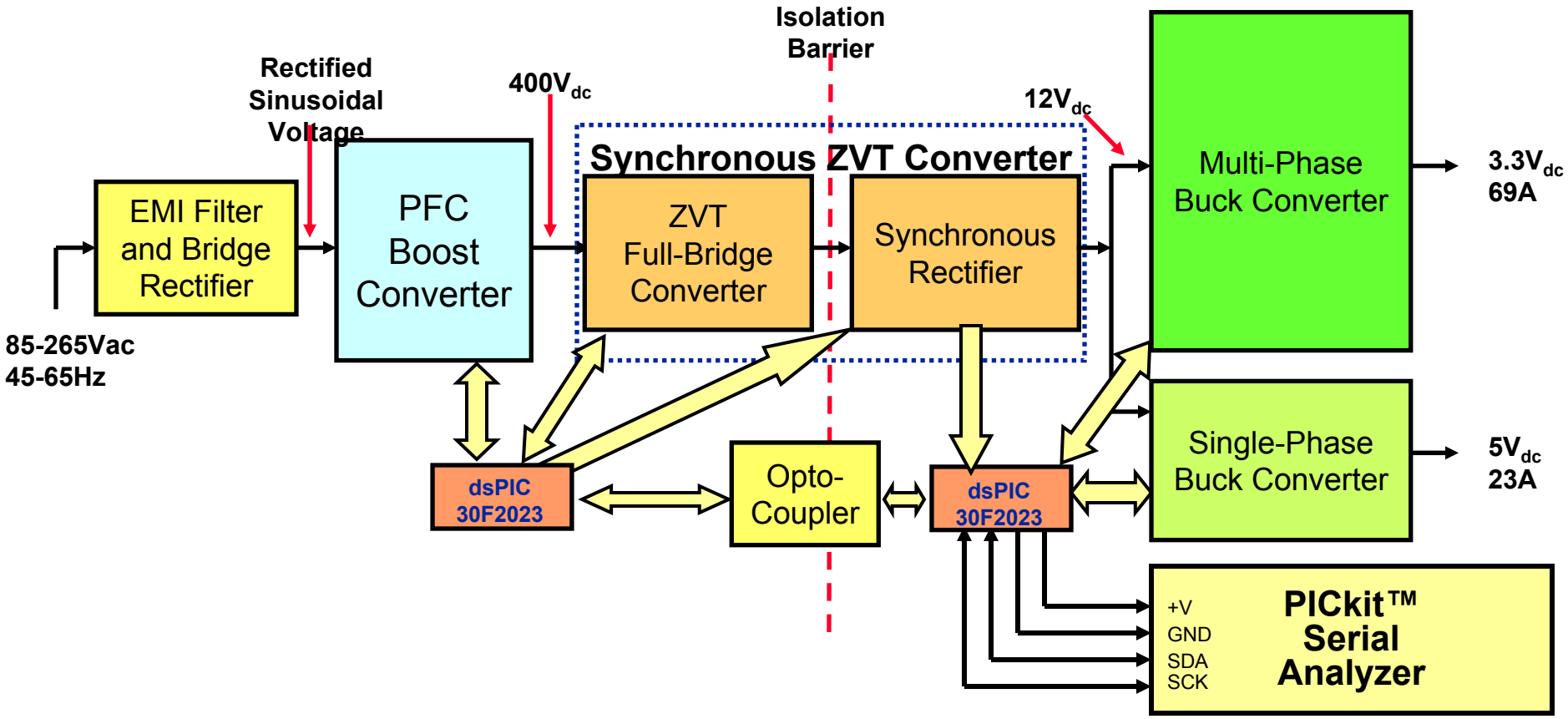
Remote Monitoring Capability



- Power monitoring can be implemented using a Serial I²C™ interface provided on the Secondary (Isolated) side

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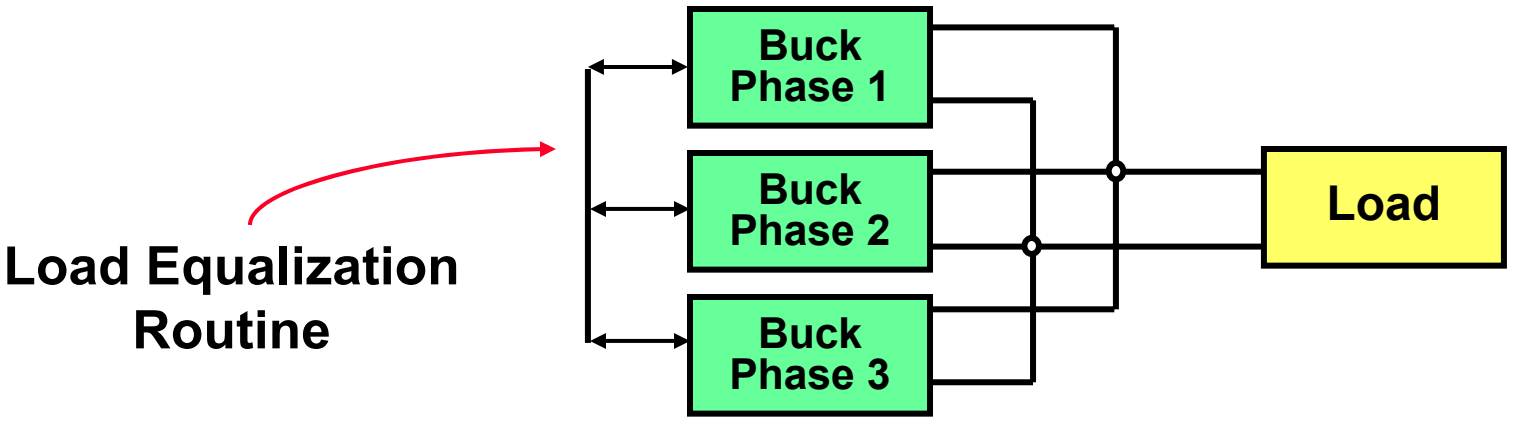
Load Sharing Issues

- Multiple power modules share load
- Component and wiring differences cause some modules to work harder than others
- The heavily loaded modules get hotter and reliability drops causing failures – Domino Effect



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Benefits of Digital Control

- Reduce Component Count
- Flexibility of Design
- Flexibility of Control
- Protect Intellectual Property
- Implement non-linear and adaptive control
- Control Multiple Stages
- Error logging capability
- Flexible Fault handling

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Summary

- **Overview of AC/DC Reference Design**
- **AC/DC Reference Design Architecture**
- **Power Factor Correction**
  - PFC Control Software
- **Zero Voltage Transition**
  - ZVT Control Software
- **Multi-phase Buck Converters**
  - Multi-phase Buck Control Software
- **Enhanced Features**

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AC/DC Reference Design

- **Availability**
  - Q4 2007
- **Contact Local Sales office for more information**
- **Visit Microchip's Intelligent Power Supply Design Center for our full product offering**
  - www.microchip.com/smps

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- L.Rossetto, G.Spiazzi, “Design Considerations on Current-Mode and Voltage-Mode control methods for Half-Bridge Converters”
- W.Gu, J.Abu-Qahouq, S.Luo, I.Batarseh, “A ZVT-PWM single stage PFC converter with an active snubber”
- M. Brown, “Power Supply Cookbook”
- M. Kazimierczuk, D. Czarkowski, “Resonant Power Converters”

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Development Tools Used in this Class

- **Hardware Tools**
  - AC/DC Reference Design (not released)
  - MPLAB® REAL ICE™ Emulator (DV244005)
  - MPLAB ICD2 (DV164005)
- **Software Tools**
  - MPLAB IDE 7.61 (SW007002)
  - MPLAB C30 v3.01 (SW006012)

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